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Novel Substrate Engineering for High Performance CMOSFETs using Channeling Ion Implantation

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1. Introduction

Multiple implantation technique is widely utilized to form a retrograde well for the scaled device. Substrate concentration increases with scale down of the feature size to maintain enough isolation characteristics. It causes the increase in junction capacitance, junction leakage and substrate constant. To realize high circuit performance, various kinds of parasitic component must be reduced in addition to increasing drive current of MOSFETs. Therefore, the reduction of junction capacitance and sheet resistance of diffusion layer is strongly required. In this paper, we propose novel substrate engineering method using a quite simple way.

2. Results and Discussion

The schematic cross section of newly developed substrate engineering is shown in Fig.1. The well profile under the STI, which determines isolation characteristics, is almost the same as conventional well profile, since the channeling phenomena is not occurred in the oxide of STI. On the contrary, the deep well with low concentration can be realized at active region by channeling implantation. Contribution of junction capacitance to the circuit performance become increase when the operation voltage is reduced. The reduction of junction capacitance is necessary for the low voltage operation with high performance.

Multiple ion implantations to form retrograde well are usually performed with the tilt angle around 7-degree to avoid ion channeling phenomena. The critical angle for ion channeling is small compared with angle deviation within a wafer. Therefore, the spatial variation within a wafer can easily be occurred for 0-degree implantation[1]. However, recently the 0-degree implantation can be available by using the parallel beam implantation with accurate angle control. Fig.2 depicts the SIMS depth profile of the active region. The well profile consists of two doping region. One is the shallow region which is formed by dechannel component during the ion penetration. The other is deeper region which is formed by channeling ions. As a result, the doping concentration around junction is reduced by using 0-degree implantation. The skew of the well boundary due to the encroachment of deep implantation and the shadowing by thick photoresist is avoided by 0-degree implantation, and inter-well isolation is improved[2]. Fig.3 shows a comparison of inter-well isolation between conventional 7-degree implantation and 0-degree implantation. 0-degree implantation is estimated to improve inter-well isolation by about 0.2um compared with 7-degree implantation. It should be noted that no degradation of intra-well isolation can be observed by 0-degree implantation, as shown in Fig.4.

The screen oxide film is generally used for the implantation. The aligned ion species in the channel direction can easily be dechanneled by this oxide film. In the case of thicker oxide film such as 15nm, the main component of well profile is formed by dechanneled ion. On the contrary, the deeper part, which is formed by channeling ions, becomes major parts of well profile in the case of thin oxide film. Therefore, the well concentration around junction can be reduced by decreasing the oxide thickness. We investigate the dependence of electrical characteristics on the oxide thickness in detail. Fig.5 shows the dependence of inter-well isolation. The inter-well isolation characteristics with 0-degree implantation can be improved compared with that of 7-degree. It should be noted that isolation characteristic shows small dependence on the oxide film thickness. Fig.6 shows Vd-dependence of junction capacitance. It is found that reduction of junction capacitance can be clearly observed in both n+/p and p+/n junction with 0-degree implantation. Junction capacitance is decreased as a screen oxide is thinner. This is due to the low concentration of impurity at the junction, which is realized by channeling ion implantation. Fig.7 shows a ratio of junction capacitance at |Vd|=1V of 0-degree implantation to that of 7-degree implantation versus thickness of a screen oxide. In the case of a screen oxide thickness is 4nm, junction capacitance of n+/p junction reduced by 15%, and that of p+/n junction reduced by 20%. Fig.8 shows a ratio of junction leakage current of 0-degree implantation to that of 7-degree implantation. The electrical field can be reduced by the low concentration well. Junction leakage current as well as junction capacitance can also be reduced by reducing oxide thickness. The reduction of junction leakage current contribute to save consumption power and to improve device characteristics, for example a retention characteristic in case of DRAM.

Fig.9 shows short channel effects of MOSFETs. A variation of threshold voltage from that of Lg=1um is same between that of 0-degree implantation and that of 7-degree implantation for both NMOSFET and PMOSFET. There are no adverse effects on characteristics of MOSFETs by channeling implantation.

We have analytically estimated tpd of a ring oscillator in the case that junction capacitance is reduced 15% for n+/p junction and 20% for p+/n junction. It is found that tpd is improved by 4% with a ring oscillator of 65nm-node (@ |Vd|=1V, Lg=35nm). Not a little improvement of a circuit performance for 65nm-node generation is easily obtained by using the simple method of channeling ion implantation.

3.Conclusion

We have studied the application of channeling implantation to form novel substrate structure. By using the 0-degree channeling implantation with thin screen oxide film, both junction capacitance and junction leakage current can be reduced without deteriorating a characteristic of MOSFETs. This newly developed substrate engineering is the one of the promising technology to realize the high performance CMOSFETs with low voltage operation.

References

[1]D.Kapila et al.,IEEE Trans. on Semiconductor Man. Vol.12, No.4 (1999), pp.457.
[2]T.Yamashita et al., Jpn. J. Appl. Phys. Vol.41 (2002),pp. 2399-2403

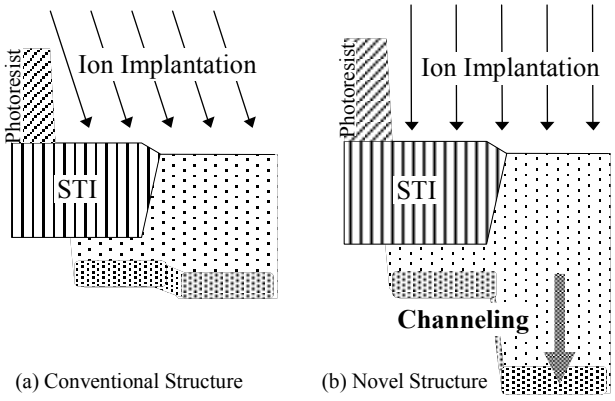

Fig.1. Retrograde well structure formed by conventional(a) and novel(b) method. Channeling is only occured in active area in the novel structure.

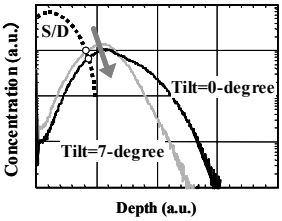

Fig.2. SIMS depth profile of retrograde well formed by 0-degree implantation and 7-degree implantation through 15nm screen oxide. Impurity concentration at metallurgical juction with source-drain diffusion is reduced in 0-degree implantation.

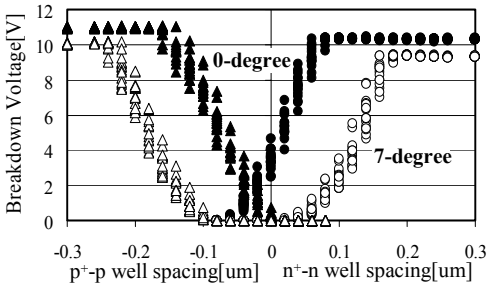

Fig.3. Comparison of inter-well isolation characteristics between 0-degree implantaion and 7-degree implantation.

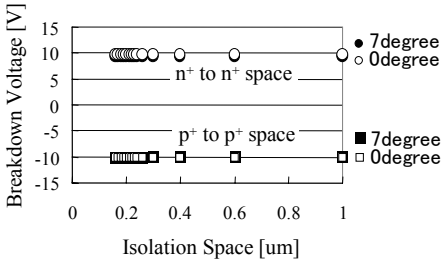

Fig.4. Intra-well Isoration characteristics.

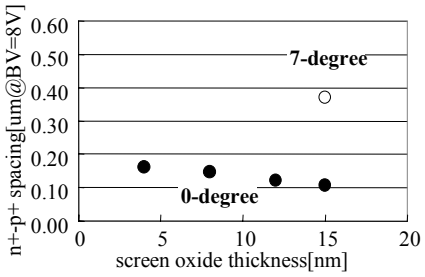

Fig.5. Dependence of inter-well isolation on a screen oxide thickness. Minimum spacing is determined by the spacing at which the breakdown voltage degrades to 8 volts.

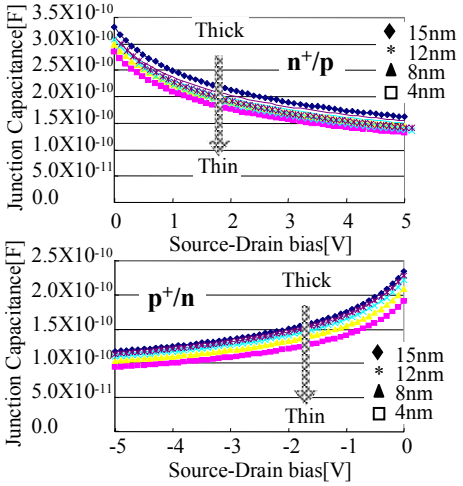

Fig.6. Source-drain bias dependence on junction capacitance. Screen oxide thickness of each curves are 4nm, 8nm, 12nm and 15nm respectively.

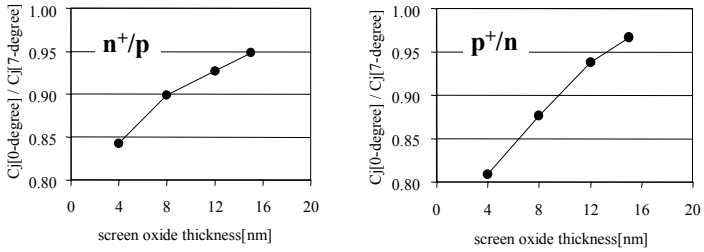

Fig.7. A ratio of junction capacitance at |Vd|=1V of 0-degree implantation to that of 7-degree implantation.

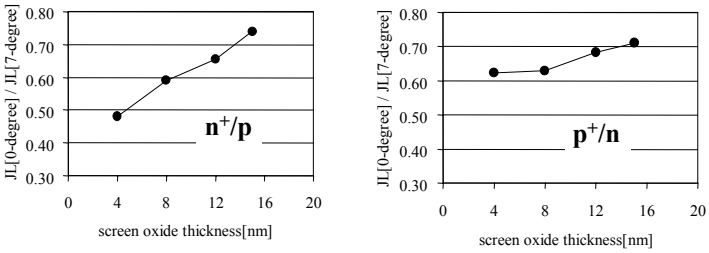

Fig.8. A ratio of junction leakage current at |Vd|=4V of 0-degree implantation to that of 7-degree implantation.

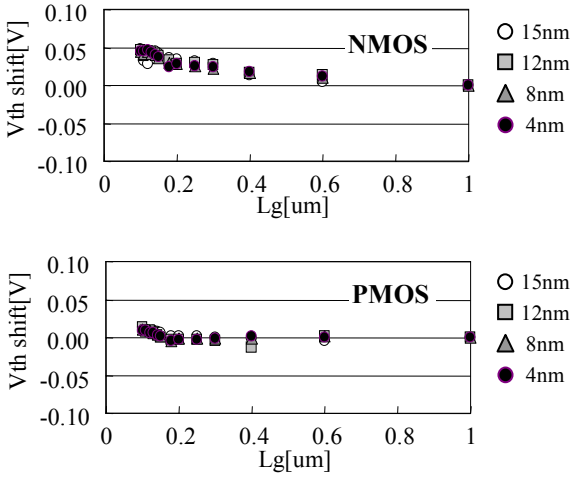

Fig.9. Shift of threshold voltage from that of Lg=1um. Although data of samples whose screen oxide thickness are 4nm, 8nm, 12nm and 15nm are plotted, they are almost coincide.