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A Variable Channel-Size MOSFET with LDD Structure

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1. Introduction

Electrical adjustment of the transfer characteristic of MOSFET is of great interest not only for developing new function circuitry but also for minimizing the circuit components. There have been proposed to electrically control MOSFET characteristic by employing the dual gate structure [1] and changing the threshold voltage with backgate bias [2]. In this work, we propose a novel MOSFET structure that can electrically alter the effective channel size. The MOSFET is named Variable Channel-Size MOSFET (VS-MOS) and can be fabricated using the conventional MOS process. Since the VS-MOS changes the effective channel size, applications which are different from the threshold-Voltage control MOSFET become possible. For example, VS-MOS can offer a continuous electrical control of logic threshold in a circuit. This characteristic can be applied to such circuits as dynamic signal-level converter and analog operation with minimal circuit size. In this paper, we report results of test fabrication and demonstrate the operation principle of VS-MOS.

2. Variable Channel Size MOSFET

A layout configuration of the prototype VS-MOS is shown in Figure 1. The VS-MOS structure features a control gate added between the main gate and the source/drain. This control gate possesses a gap Sc at the end. The control gate can modulate the effective channel size through the control gate voltage Vcg. The channel-size modulation property of this device is explained from the device simulation results shown in Figure 2 where the potential (0.1 V step contour) at the surface of the VS-MOS and the current (direction and size of arrows) are plotted. When Vcg=3.0 V, the main gate voltage Vg=3.0 V, and drain voltage Vd=3.0 V (Fig. 2(a)), the potential slope is almost vertical against the main gate since the resistance under the control gate is sufficiently low. In this case, the main gate size has a shape very similar to the conventional MOSFET. When Vcg is set to be zero to turn-off the control gate while keeping Vg=Vd=3.0 V (Fig. 2(b)), the current concentrates at the gap Sc at the end of the control gate. This causes the potential slope become diagonal to the main gate. As the result, the effective channel length becomes large and the effective channel width becomes small. Thus, the VS-MOS achieves continuous modulation of effective channel size by controlling the voltage Vcg. The modulation characteristic is determined by the shape parameter L, W, Lc, Sc & Sv values defined in Figure 1 and the Sv diffusion resistance value.

3. Fabrication of test device

Many VS-MOS test device prototypes were measured to study the relation between the VS-MOS shape parameter and channel size modulation properties. These evaluations involved the trial production of devices using a normal CMOS manufactured process at a minimum line width of 1.0 μm and 0.35 μm respectively.

The test devices fabricated with 1.0 μm CMOS technology are gate width W=5, 10, 20 μm, L=1.5 μm, Lc=Sc=Sv=1.0 μm. The test devices fabricated with 0.35 μm CMOS technology are gate width W=3.5, 7.0, 14 μm, L=0.35 μm, Lc=Sc=Sv=0.35 μm, Sc=0.5 μm. In the 0.35 μm devices, Lightly Doped Drain (LDD) structure was employed. Figure 3 shows schematic cross-section of the LDD VS-MOS. The LDD VS-MOS enables an impurity concentration for the diffusion region Sv between the main gate and control gate to be formed lower than the source/drain region. The channel size modulation is expected to become pronounced with employing LDD, since the increase in resistance at Sv region results in increase of the potential drop along the gate width.

Figures 4 and 5 show photomicrographs of the prototype 1.0 μm and 0.35 μm VS-MOS transistors.

4. Measurement Results

Figure 6(a) shows the variation of Vg-Id characteristic of the p-type 1.0 μm VS-MOS (L=1.5 μm, W=20 μm, Lc=Sc=Sv=1.0 μm) with Vcg from 0.0 V to 3.0 V in 0.3 V increments under Vd=3.0 V. Figure 6(b) shows the results obtained from the n-type 0.35 μm VS-MOS (L=0.35 μm, W=7.0 μm, Lc= Sv =0.35 μm, Sc=0.5 μm). We can clearly see that the transfer characteristic is controlled by changing the control gate Vcg.

Figure 7 shows the experimental and simulation results for Id modulation ratio with a W/Sv difference. From these results, we confirm that the Id modulation ratio increases with increasing W/Sv and the Sv diffusion resistance.

Figure 8 shows the measurement results of Input-Output characteristic of a VS-MOS inverter. We can see that modulation extent of 0.35 μm VS-MOS with LDD structure is larger than 1.0 μm VS-MOS.

5. Summary

A Variable Channel-Size MOSFET was proposed and fabricated using the conventional CMOS process. It was confirmed that the channel size modulation property can be designed by adjusting the shape parameters by evaluation of the test devices. The channel size modulation ratio can be large by employing LDD structure. The VS-MOS of L/W=0.35/14.0 μm with LDD structure can achieve a Id modification ratio of 99%.

Acknowledgment

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References

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[2] T.Hiramoto and M.Takamiya, *IEICE Transactions on Electronics, Vol.E83-C, No. 2*, pp. 161-169, February, 2000.

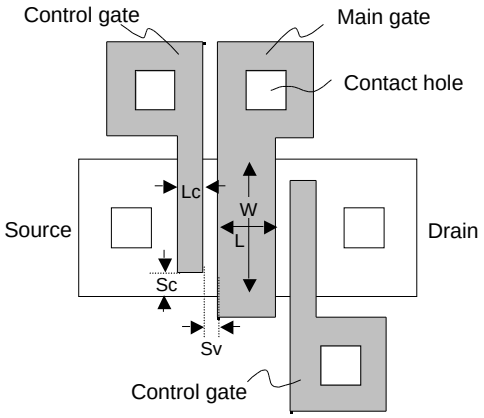


Fig. 1 Layout of VS-MOS

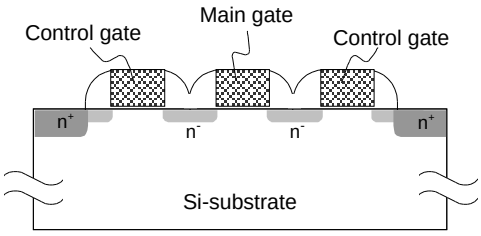


Fig. 3 Schematic cross section of VS-MOS employed LDD

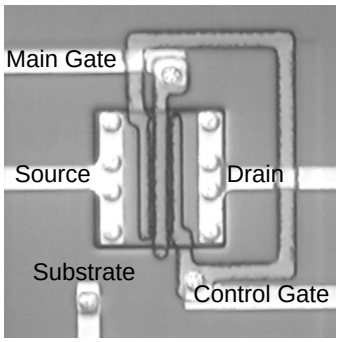


Fig. 4 Photomicrograph of a 1.0 μmVS-MOS (W=20 μm, L=1.5 μm, Lc=Sv=Sc=1.0 μm)

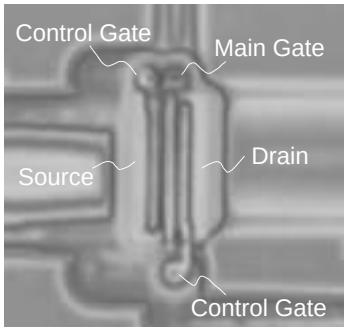
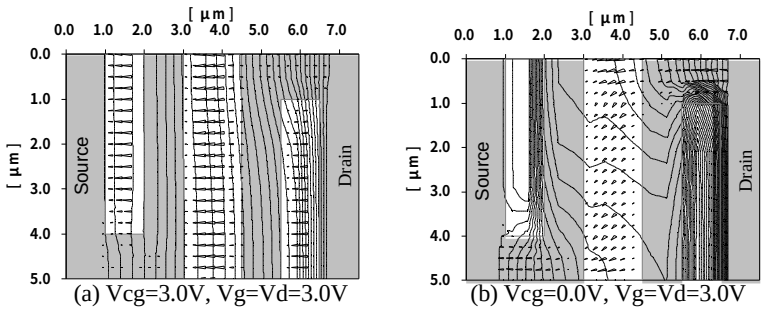
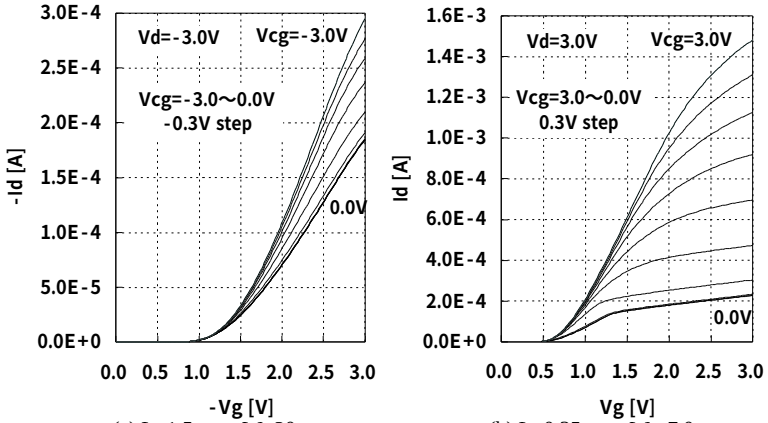


Fig. 5 Photomicrograph of a 0.35 μmVS-MOS (W=7.0 μm, L=Lc=Sv=0.35 μm, Sc=0.5 μm)



(a) Vcg=3.0V, Vg=Vd=3.0V (b) Vcg=0.0V, Vg=Vd=3.0V

Fig. 2 Simulation results for potential and current in a VS-MOS



(a) L=1.5 μm, W=20 μm, Lc=Sv=Sc=1.0 μm

(b) L=0.35 μm, W =7.0 μm, Lc=Sv=0.35 μm, Sc=0.5 μm

Fig. 6 Measurement result of Vg-Id characteristic of a VS-MOS

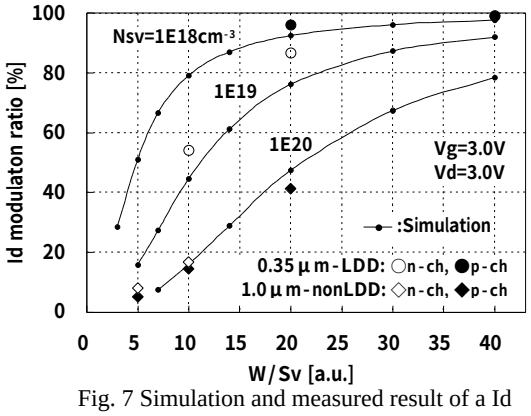
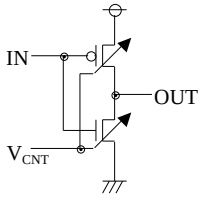
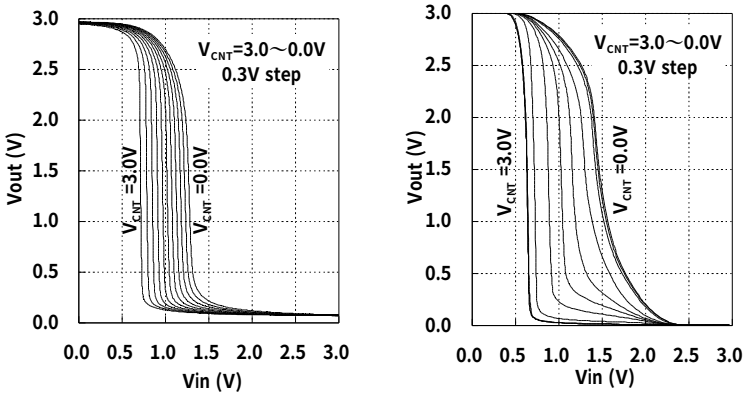


Fig. 7 Simulation and measured result of a Id modulation ratio as a function of W/Sv.



VS-MOS inverter



(a) L=1.5 μm, Wp/n=10/10 μm, Lc=Sv=Sc=1.0 μm

(b) L=0.35 μm, Wp/n=7.0/3.5 μm, Lc=Sv=0.35 μm, Sc=0.5 μm

Fig. 8 Measurement result of Input-Output characteristic of a VS-MOS inverter