A New One-Transistor One-Bipolar (1T1B) Capacitor-Less DRAM Cell

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1. Introduction

As the device feature size scales down to deep sub-100nm regime, Dynamic Random Access Memory (DRAM) is severely limited by off-state leakage for data retention and storage node capacitance for sufficient signal to noise ratio [1]. It is well known that off-state leakage cannot be easily reduced due to the theoretical 60mV/decade limit of sub-threshold swing at room temperature. In order to obtain reasonable cell capacitances, advanced technologies such as high dielectric materials and/or complex storage node formation technology are necessary.

In order to overcome these limitations, several capacitor-less memory cells have been proposed to replace the conventional DRAM cell [2]-[4]. In these cells, the impact ionization mechanism is utilized to change the bulk potential, resulting in an increase of writing time since the hole current generated by the impact ionization is much smaller than that of drain current. In this paper we propose a new DRAM cell structure incorporating One Access Transistor and One Bipolar transistor (1T1B) to achieve simple and high speed memory cell operations.

2. Cell structure

Fig. 1 shows the cross-section of the memory cell and its equivalent circuit. The cell consists of one access transistor with recessed gate (VWL) and one merged bipolar transistor to increase the writing speed of the cell. The T-gate structure allows flexible bipolar optimization. The n-doped storage node is formed on the p-type substrate and the n' drain of the access transistor (VCC) is isolated from the storage node by the oxide below the n' drain region. The unit cell area of this cell is 8F^2 (F: minimum feature size).

3. Cell operation

The two-dimensional device simulator, SILVACO, with calibrated impact ionization parameters from the measurement data [5] is used for simulation throughout this study.

There are three memory operations: READ, WRITE and HOLD. The applied voltages for the operations are listed in Table. 1 and will be used in the subsequent discussions.

In order to obtain a successful read operation, a measurable difference in access transistor currents is necessary. This can be obtained by changing the access transistor threshold voltage which is a function of the storage node voltage as shown in Fig. 2. When the storage node is stored with “1”, the threshold voltage of the access transistor is lower than that of “0” due to the bulk depletion charge sharing effect of the back gate. This leads to a measurable difference in drain currents for the 80nm gate length access transistors. This difference in drain currents allows the sensing of the information stored in the storage node during READ operations. After successful reading by the sense amplifier, the bit line voltage (VBL) is automatically restored in the storage node as long as the word line voltage is high (Refresh operation).

In WRITE operation, data (charge) is stored in the storage node through the impact ionization followed by the bipolar action as the hole current due to the impact ionization becomes the base current of the npn bipolar transistor formed vertically below the source region (V_Bi). High current gain of bipolar transistor enables fast writing speed.

When “0” is stored, the bit line voltage (VBL) is set to “0”. When “1” is stored, however, VBL is set in the middle of the operation voltage, VCC/2 in this study since voltage difference between VCC and V_Bi is necessary for hole injection into the bulk to activate the bipolar transistor.

Fig.3 shows the storage node voltage changes as a function of writing time after a VWL of 2V is applied for WRITE “1”. In this simulation, a 10F cell capacitor is connected to the storage node to magnify the writing speed as inserted in Fig. 3. Fig. 4 shows the storage node voltage changes as a function of writing time for WRITE “0”.

Fig.5 shows the comparison of writing speed between cells with and without bipolar transistor. The cell without bipolar transistor represents the previous cells proposed in the past [2]-[4]. It is noticeable that there is a significant improvement of writing speed in the cell with bipolar transistor due to bipolar transistor current. This implies that the proposed 1T1B DRAM cell is suitable for high speed DRAM operations.

4. Proposed process flow

Fig. 6 shows the proposed process sequence for the memory cell formation. After active region formation (Fig. 6b), silicon epitaxial layer is filled in the active region using CMP technology (Fig. 6d). T-gate formation is then performed and followed by conventional transistor process to complete the cell structure. A detailed process sequence is listed in Fig. 6.

5. Conclusions

In this paper, a new capacitor-less DRAM cell concept for future memory cell applications is proposed. The cell consists of one access transistor and one bipolar transistor. Using device simulation, it is demonstrated that the new memory cell shows higher writing speed than that of the single transistor type capacitor-less memory cell proposed in the past. This cell, therefore, is a highly promising DRAM structure for deep sub-100nm regime.

References

Fig. 1 Cross-section and equivalent circuit of the cell

(a) Cross-section of the cell    (b) Equivalent circuit

Table 1: Applied voltages used in simulation

<table>
<thead>
<tr>
<th>Condition</th>
<th>$V_{CC}$</th>
<th>$V_{BL}$</th>
<th>$V_{WL}$</th>
</tr>
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<tbody>
<tr>
<td>READ</td>
<td>2 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WRITE &quot;0&quot;</td>
<td>2 V</td>
<td>0 V</td>
<td>2 V</td>
</tr>
<tr>
<td>WRITE &quot;1&quot;</td>
<td>2 V</td>
<td>1 V</td>
<td>2 V</td>
</tr>
<tr>
<td>HOLD</td>
<td>2 V</td>
<td>0~2 V</td>
<td>0 V</td>
</tr>
</tbody>
</table>

Fig. 2 I-V characteristics for “0” state and “1” state in the storage node.

Fig. 3 Potential variation as a function of writing time for WRITE “0”.

Fig. 4 Potential variation as a function of writing time for WRITE “1”.

Fig. 5 Comparison of writing speed for memory cells with and without bipolar transistor.

Fig. 6 Proposed process flow for the cell fabrication.