Novel Storage-Node Contacts with Stacked PCM-Sp-TiN Barrier for MIM-Ru/Ta2O5/Ru Capacitors in Giga-Bit DRAMs

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1. Introduction
The MIM-Ru/Ta2O5/Ru capacitor with a TiN barrier (Fig. 1) is the most promising in giga-bit DRAMs with design rules of 0.10 μm and below, because CVD processes of Ru, Ta2O5, and TiN have been matured for mass productions. However, the TiN barrier is easily oxidized during an annealing process for reducing the leakage current of the Ta2O5 film (Fig. 2) [1]. This oxidation increases the contact resistance (Rc) of the Ru storage node (SN) and the TiN barrier, and causes a serious problem in DRAM high-speed operations.

In this study, we have investigated the dependence of the Rc on the characteristics of the TiN barriers. Based on the results, we have proposed novel Ru/TiN contacts with a stacked-barrier (SB) structure fabricated by using the point-cusp magnetron (PCM) sputtering technique.

2. Contact Resistance & Characteristics of TiN Barrier
For analytical study, we used test structures with TiN barriers deposited by various methods (Fig. 2). The sp-TiN barrier was deposited by a prevalent reactive sputtering method using a Ti target in N2/Ar ambient. Two types of CVD-TiN barriers were deposited by using Ti[N(CH3)2]3 (TDMAT) as a source gas: one with a plasma nitridation during the deposition, and the other without a nitridation. The Rc was measured by applying -1 to +1 V between the Ru SN and the TiN barrier (Fig. 2). A high Rc with non-ohmic characteristics was obtained for the CVD-TiN barrier after the oxidation annealing, although a low Rc with ohmic characteristics was obtained for the sp-TiN barrier (Fig. 3a). The TEM-EDX spectra revealed that the titanium oxide (TiOx) was formed at the Ru/Ti interface, and that the TiOx thickness increased along with the Rc (Fig. 3b). Furthermore, the X-ray photoelectron spectra revealed that the Ti/N ratio in the TiN barriers also varied with the TiN deposition methods (Fig. 3c). Thus, the Rc as well as the TiOx thickness is strongly related with the Ti/N ratio (Fig. 4). The TiOx is supposed to be easily formed from the excess amount of Ti in the TiN barriers, and to increase the Rc.

Accordingly, the Ti/N ratio should be controlled to keep the Rc low. The CVD-TiN always involves the excess Ti, because the CVD process is consisted of two process steps: a deposition of a Ti rich layer, and a plasma treatment for nitridation. On the other hand, the sp-TiN cannot fill the contact holes with a high aspect shown in Fig. 1. Thus, we propose a novel SB structure with a sp-TiN barrier fabricated by using the PCM sputtering method (Fig. 5). By this method, the Ti/N ratio can be easily controlled by the sputtering ambient of N2/Ar gas mixture.

3. Device Integration & Electrical Properties

Device Integration
The MIM-Ru/Ta2O5/Ru capacitors with the SB structure were integrated according to the process flow in Fig. 6. The contact holes with diameters of 0.10 μm were opened by an RIE process, and the sp-TiN film was deposited on the sidewall. The Rc of the Ru SN and the plug-structured TiN barrier (Fig. 2) varied with the structure of the TiN barriers. The Rc has non-ohmic characteristics (Fig. 10b) with a larger dispersion (Fig.11). In addition, the Rc for the conventional structure varied with the structure of the TiN barrier. The Rc of the Ru SN and the plug-structured TiN (see Fig. 1) was 100 times larger than the Rc of the Ru SN and the "flat" TiN (see Figs. 2 and 3a). We suppose that an insufficient nitridation in the contact holes causes an excess Ti and an increase in the Rc for the plug-structured barrier.

A low resistive contact of 30 kΩ-bit was obtained even after an annealing at 460°C for the SB structure (Fig. 12), so that the Ta2O5 film can be enough oxidized to reduce the leakage current. The leakage current obtained was below 1E-16A/bit (-1 to +1 V) (Fig. 13). This value is sufficient for the giga-bit scale DRAM applications.

4. Conclusions
We have developed the novel stacked barrier structure by using the PCM sputtering technique. With this structure, we have obtained the contact resistance of 10kΩ-bit and the leakage current of 1E-16A/bit (-1 to 1 V).

References
Fig. 1 Schematic view of MIM-Ru/Ta2O5/Ru capacitor with conventional structure.

Fig. 2 TEM view of the Ru/TiN interface after oxidation. Oxygen diffused through Ru and oxidized TiN.

Fig. 3. Rc, TiOx thickness, and Ti/N ratio for TiN deposited by various methods.

Fig. 4 Rc and TiOx as function of Ti/N ratio.

Fig. 5 Schematic view of MIM-Ru/Ta2O5/Ru capacitor with SB structure.

Fig. 6 Process flow to fabricate Ru/Ta2O5/Ru capacitor with SB structure.

Fig. 7 SEM view of deposited PCM-barrier.

Fig. 8 SEM view after removal of Ru and TiN by using multi-step etching.

Fig. 9 (a) SEM and (b) TEM views of MIM-Ru/Ta2O5/Ru capacitor with SB structure.

Fig. 10 I-V characteristics of (a) SB and (b) conventional structures.

Fig. 11 Distribution of Rc for SB and conventional structures.

Fig. 12 Rc as function of oxidized temperature in O3 for SB and conventional structures.

Fig. 13 I-V characteristics of concave-type MIM-Ru/Ta2O5/Ru capacitor with SB structure.