Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 474-475

P3-13

Defect Generation in Gate Oxide by Selective Oxidation in Hydrogen-rich Wet Ambient

Heung-Jae Cho, Kwan-Yong Lim, Se-Aug Jang, Jung-Ho Lee, Jae-Geun Oh, Yong-Soo Kim, Hong-Seon Yang, and Hyun-Chul Sohn
Memory R&D Division, Hynix Semiconductor Inc., Ichon P.O. Box 1010, Ichon-si, Kyoungki-do 467-701, Korea
(Phone: +82-31-630-4466, Fax: +82-31-630-4545, e-mail: heungjae.cho@hynix.com)

INTRODUCTION

W/poly-Si gate has gradually drawn attraction for the low resistivity with the shrink of devices. One of the problems in the W/poly-Si gate is the abnormal oxidation of W during conventional gate reoxidation in O_2 ambient. The selective oxidation (SO) process performing in high temperature H_2-rich H_2O ambient is considered to be the solution, because the Si is selectively oxidized. The high temperature hydrogen-rich process, however, is reported to degrade the electrical characteristics of gate oxide due to the defect creation by atomic hydrogen in the oxide [1].

In this paper, we report the effect of SO process on the degradation of oxide in terms of stress induced leakage current (SILC), oxide trap, and interface state density (D_{it}).

EXPERIMENTAL

In this experiment, the W film was not employed in order to exclude issues of W contamination. n+Poly-Si(1500Å)/SiO_2 (55Å)/Si nMOS capacitors with shallow trench isolation (STI) were fabricated on the p-type (100) Si substrate (8-inch dia.). After gate patterning, gate reoxidation was carried out in H_2-rich H_2O ambient at high temperatures from 850℃ to 950℃. Some samples were re-oxidized at 850℃ in furnace (FO) or RTP system (RTO) in O_2 ambient for comparison. Post N_2-annealing processes were then performed in a furnace (150min at 710℃) and RTP system (10sec at 1000℃), followed by H_2/N_2 forming gas anneal. The area of MOS capacitors evaluated was $100\times100um^2$.

RESULTS AND DISCUSSION

Shown in Fig. 1 are the J-V curves measured before and after stress of $-1C/cm^2$. The fresh devices have almost identical leakage current regardless of reoxidation conditions. After stressing, the sample re-oxidized at 950℃ in H_2-rich H_2O ambient with the post anneal (SO w/ PA) shows seven times higher SILC at –4.9V than that of the furnace oxidation one with the post anneal (FO w/ PA). The SO sample without the post anneal (SO w/o PA) displays increase of SILC by more than 1 order of magnitude. Fig. 2 exhibits the normalized leakage current increase as a function of injected charge. It is noted that the defect generation rates, i.e. the slop of the linear region before saturation, of SO samples are faster than that of FO w/ PA sample. The leakage increase of FO w/ PA is more rapidly saturated compared to those of SO samples. The SO w/o PA sample shows the highest leakage current, and the FO w/ PA sample displays the lowest.

In order to understand the higher SILC and more defect generation in the SO samples, we measured the C-V hysteresis (+3V -> -3V -> +3V) before and after stress of $-1C/cm^2$. All fresh devices show no hysteresis. After the electrical stress, however, hysteresis and decrease of accumulation capacitance are observed, suggesting the generation of oxide trap by electrical stress. The C-V curves also show the negative shift of V_{fb} and the non-ideal hump, indicating that abnormal positive charges and interface defects were created in the oxide and at the SiO_2/Si interface with the stress, respectively. Especially both SO samples show a serious distortion in C-V curves such as higher hysteresis, hump region, and abnormal shift of Vfb. Fig. 4 shows stress induced slow trap density (N_{ot}) in oxide calculated from the area of C-V hysteresis shown in Fig. 3 [2]. The SO w/o PA has the highest N_{ot}, whereas the FO w/ PA exhibits the lowest N_{ot}. These trends are well consistent with those of SILC and defect generation. Fig. 5 exhibits the conductance loss (G/ω)-$\log\omega$ plots of MOS capacitors measured after stress of $-1C/cm^2$ to characterize interface state density. The D_{it} calculated from the maximum conductance loss peak is plotted before and after the electrical stress in Fig. 6. There is no difference in D_{it} level, medium $10^{10}eV^{-1}cm^{-2}$, for all the fresh samples. After the stress of $-1C/cm^2$, as one can infer from the non-ideal C-V hump, it displays a distinct difference; FO w/ PA has the lowest D_{it} level (about $1\times10^{11}eV^{-1}cm^{-2}$), and SO w/o PA does the highest ($5\times10^{11}eV^{-1}cm^{-2}$).

By hydrogen release model [3], the hydrogen released from anode interface induced by the electrical stress diffuses through oxide, interacts with the point defects, and creates additional trap sites. It is also reported that the high temperature anneal above 500℃ in H_2 ambient can introduce atomic hydrogen to not SiO_2/Si interface but also oxide bulk, and the hydrogen may react with Si dangling bond, strained Si-Si and/or Si-O bonds to form additional Si-H bond [1,4]. Therefore, it is expected that excess hydrogen species in oxide introduced by the SO step, high temperature hydrogen process, are easily released from SiO_2/Si interface and oxide bulk under F-N stress due to a low Si-H binding energy of about 0.3eV. The released atomic hydrogen subsequently increases defect generation such as D_{it} and oxide trap density, resulting in degradation of the SILC. The diffusion-out of hydrogen from the SiO_2/Si interface and oxide bulk during the post anneal is considered as one of the origins of the improved electrical characteristics of the MOS capacitor with post anneal process after SO.

To investigate the SO temperature effect on defect generation, the N_{ot} and D_{it} of MOS capacitors with different SO temperatures from 850℃ to 950℃ were probed as show in Fig. 7 (a) and (b), respectively. The sample re-oxidized in O_2 ambient with RTP (RTO) is also plotted for comparison. The RTO sample has the lowest N_{ot} and D_{it} which are similar to those of FO sample shown in Fig. 4 and Fig. 6. In the SO samples, the N_{ot} and D_{it} increase with increasing SO temperature. These indicate that with increasing SO temperature, the hydrogen species are more uniformly distributed across the oxide and then react with defects such as dangling and strained bonds, resulting in increased defect generation under the electrical stress.

CONCLUSION

We studied the effect of selective oxidation on gate oxide reliability. The SO process carried out in high temperature H_2-rich H_2O ambient was found to generate defects both at SiO_2/Si interface and in oxide bulk, and degrade the SILC characteristics. Devices with gate reoxidation in conventional O_2 ambient showed better characteristics. The decreased SO temperature and additional post anneal processes were also observed to reduce the SILC, oxide trap, and interface state density.

REFERENCES

[1] Y. Nissan-Cohen *et al*., *IEEE EDL*, ***9***, 287 (1988).
[2] D. M. Fleetwood *et al*., *J. Appl. Phys.*, ***79***, 1583 (1996).
[3] D. J. DiMaria *et al*., *J. Appl. Phys.*, *73*, 3367 (1993).
[4] L. Do Thanh *et al*, *J. Electrochem. Soc*., **135**, 1797 (1988).

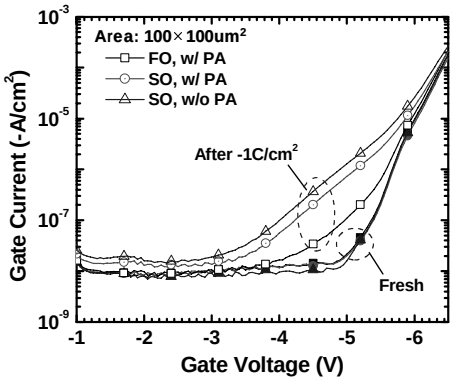

Fig. 1. J-V curves of various samples before and after electrical stress. Maximum stress induced leakage current (SILC) is monitored at about -4.9V.

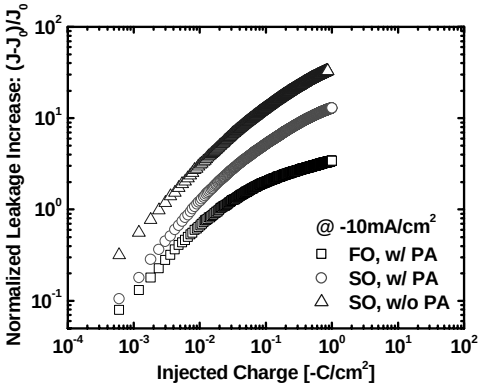

Fig. 2. Normalized gate leakage current vs. injected charge plot, where the sensing voltage was -4.9V. (J_0: gate current before stress, J: gate currents monitored after charge injection)

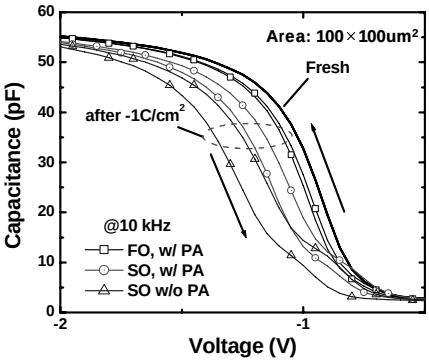

Fig.3. C-V hysteresis curves (+3V -> -3V -> +3V) of various samples before and after electrical stress. All fresh devices showed no hysteresis.

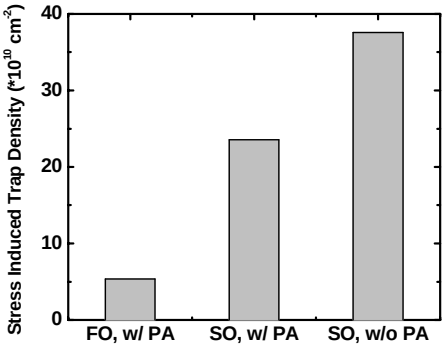

Fig. 4. Stress induced slow trap density calculated from the C-V hysteresis of the stressed devices shown in Fig. 3.

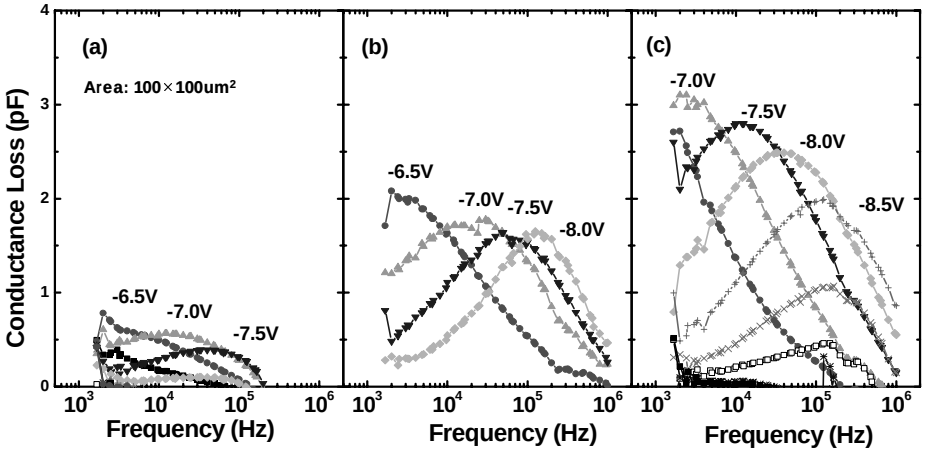

Fig. 5. Conductance loss (G/ω) -log ω plots of various MOS capacitors after -1C/m², (a) FO w/ PA, (b) SO w/ PA, and (c) SO w/o PA.

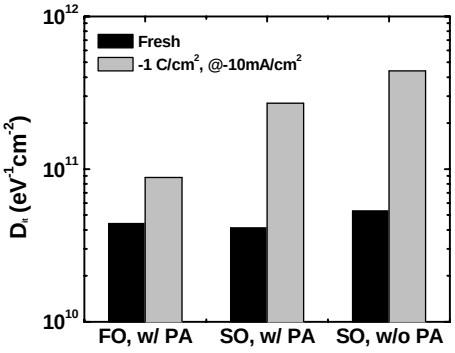

Fig.6. Comparison of interface state density before and after stressing. The D_{it} was calculated from the maximum conductance loss peak shown in Fig. 5.

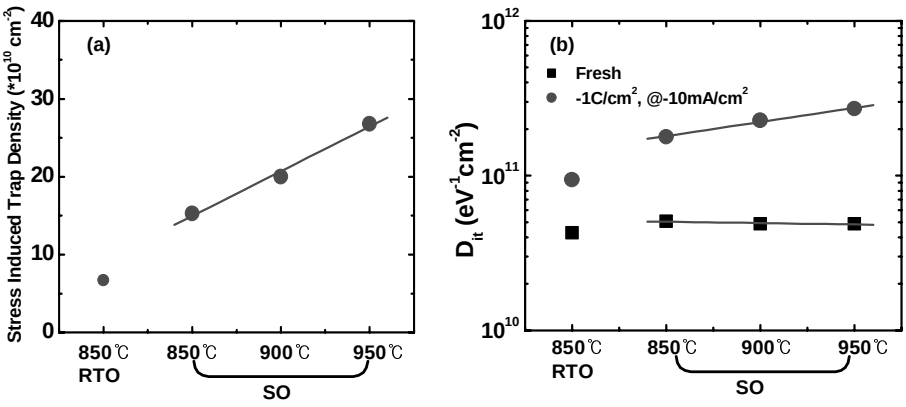

Fig.7. Effect of selective oxidation temperatures on the (a) stress induced slow trap density and (b) interface trap density.