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Improving Electrical Properties of CVD HfO_2 by Multi-Step Deposition and Annealing in a Gate Cluster Tool

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1. Introduction

Reduction of gate leakage current by orders of magnitude has been demonstrated by HfO_2 [1], but successful integration of HfO_2 into the conventional CMOS process remains a challenge due to its thermal instability [2]. Study has shown that HfO_2 easily crystallize at low temperature [3] and the incorporation of carbon into the high-K material during CVD process causes desorption of C-O bonds at high temperature annealing which eventually leads to pinholes formation [4]. These deteriorate the device performance as it results in high leakage current. It is therefore essential to improve thermal stability of HfO_2. In this work, we attempt to reduce leakage current after high temperature annealing by 'blocking' the direct leakage current path caused by grain boundaries and pinholes. The final gate stack consists of multi-layers HfO_2 with each layer deposited and annealed independently in a cluster tool so as to 'offset' the grain boundaries and pinholes from one layer to another.

2. Experiment

The MOS capacitor fabrication process flow is shown in Table 1. HfO_2 was deposited in a MOCVD system using $Hf(OC(CH_3)_3)_4$ [Hf "t-butoxide"] precursor at 400°C with O_2 flow. For multi-step deposition, each step consists of deposition of HfO_2 of certain thickness, followed by post deposition annealing (PDA) in a N_2 ambient at 700°C for 60sec. This 'deposition followed by PDA' step is repeated on top of the previously deposited and annealed HfO_2 until a final gate dielectric of desired physical thickness is formed. Fig. 1 illustrates the basic idea of multi-step deposition, suggesting that the grain boundaries and pinholes are offset from one layer to another to 'block' the direct leakage path. To avoid undesirable contamination between the multi-layers of HfO_2, the multi-step deposition and PDA was done in a cluster tool so that all the wafer transportation and process could be done without a break of controlled ambient. To evaluate thermal stability of the films, RTA of 950°C was implemented either before or after TaN electrode deposition.

3. Results and Discussion

Fig. 2 shows the physical thickness variations during the single-step deposition process as well as the multi-step (double-step/quadruple-step) deposition process for HfO_2. During PDA, the decrease of thickness due to densification of HfO_2 film and the increase of thickness due to growth of the bottom interfacial layer (IL) happen together. Therefore, the smaller decrease after PDA in a certain step compared to others in Fig. 2 indicates more IL growth during that particular step. It can be seen from Fig. 3 that the reduction of HfO_2 thickness after PDA for each step (Δt_{OX}) is almost constant when the surface nitridation was done before HfO_2 deposition. This indicates that there is no excessive growth of IL even though PDA steps were repeated during multi-step deposition, and that there is no further densification of the film during the subsequent PDA once the earlier deposited layer already went through PDA. Fig. 4 shows the high-frequency C-V for multi-step and single-step deposited HfO_2 with surface nitridation. Excellent agreement with simulated C-V curve indicates that the repeated cycle of deposition and PDA does not cause any degradation of interfacial quality. Fig. 5 shows the leakage current versus EOT of HfO_2 prepared by single and multi-step deposition. Leakage current with surface nitridation shows a parallel trend with SiO_2 benchmark data [5], which indicates that the multi-step deposition does not degrade the leakage current performance. However, without surface nitridation, multi-step deposition has a higher gradient in the figure which indicates the degradation of leakage current by repeated PDA. Figure 6 compares C-V and IV of single and double-step deposited HfO_2 films after RTA at 950°C. The two films have nearly identical C-V curve as seen in the inset of Fig. 6, which means the same EOT and V_{FB}. However, the double-step deposited HfO_2 exhibits lower leakage current by more than 1 order of magnitude compared to single step deposited HfO_2 when the two films underwent the same high temperature process, demonstrating the successful offset of grain boundaries and pinholes leading to 'blockage' of leakage path. Thermal stability of HfO_2 with top metal electrode TaN was also investigated, by applying RTA after the formation of TaN electrode. As can be seen in Figs. 7 and 8, the increase in J_g and EOT after RTA depends on the number of steps involved in depositing the entire HfO_2 dielectric. The more steps employed the smaller increase in leakage current and EOT after RTA. This implies that HfO_2 film prepared by multi-step deposition reacts less with TaN metal gate because of its improved thermal stability.

4. Conclusion

We have successfully demonstrated the feasibility of multi-step deposition technique using MOCVD cluster tool. We have shown that multi-step deposition of HfO_2 shows improved thermal stability after high temperature annealing of 950°C, for both before and after metal gate deposition compared to conventional single-step deposition.

References

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- Field oxidation and active patterning
- RCA cleaning and HF (1:100) dip
- Surface nitridation: NH_3, 700°C
- **Multi-step deposition in MOCVD cluster tool**
- Rapid thermal annealing (RTA): 950°C, N_2, 30 sec (or skip)
- TaN deposition: 3mT, 400W
- Rapid thermal annealing (RTA): 950°C, N_2, 30 sec (or skip)
- Gate patterning
- Anneal at 420°C, 10 mins in a H2/N2 ambient

Table 1. Fabrication process of MOS capacitor.

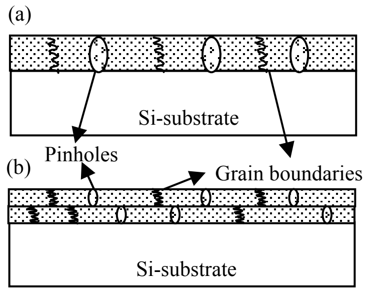

Fig. 1. Schematic drawing of the idea on how multi-step deposition can improve leakage current after annealing. (a) single-step deposition and (b) offset of leakage current path by double-step deposition of HfO_2.

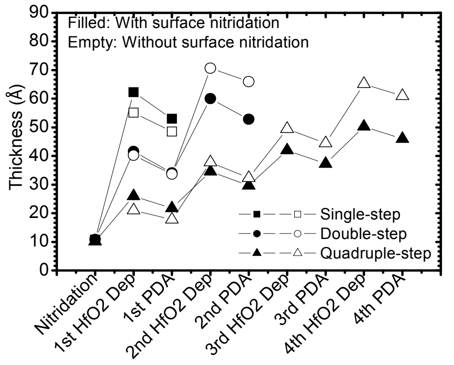

Fig. 2. Single-step deposition involves one time deposition of HfO_2 followed by PDA while multi-step (double/quadruple-step) deposition is cycles of single-step deposition (2/4 cycles). Thickness variation after PDA is a combination of decrease by densification and increase by IL growth.

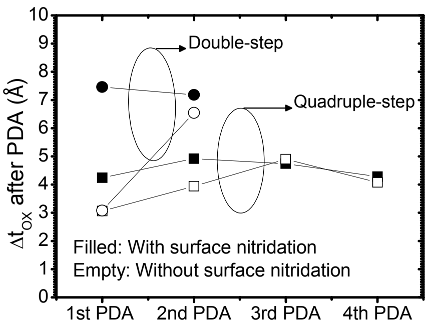

Fig. 3. Variation of Δt_{OX} during the multi-step deposition. Constant Δt_{OX} , when the surface nitridation was done, indicates that there is no excessive growth of IL even though PDA steps were repeated.

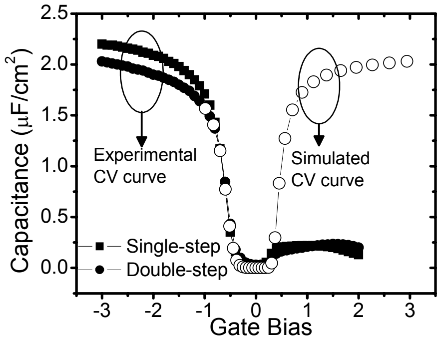

Fig. 4. Good fitting between simulated CV curve and experimental CV curves, indicating good interfacial quality and no increase in D_{it} by repeated PDA.

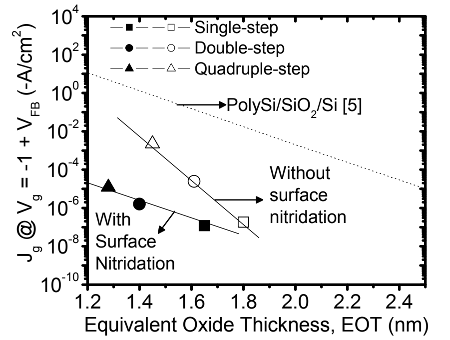

Fig. 5. Multiple-step deposited HfO_2 on nitrided substrate shows parallel trend with benchmarked SiO_2 data, indicating that multi-step deposition does not degrade leakage current of as-deposited HfO_2 film.

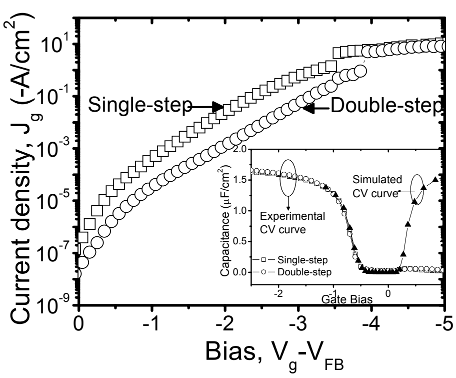

Fig. 6. Multi-step deposited HfO_2 shows lower leakage current compared to single step deposited HfO_2 after RTA of 950°C. Inset shows similar V_{FB} and EOT of 17Å after RTA for both films.

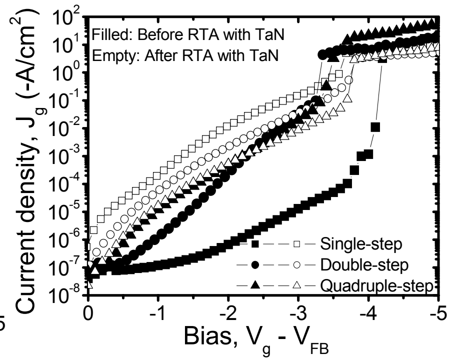

Fig. 7. Leakage current before and after RTA of HfO_2 with TaN gate. The RTA was done after TaN gate formation.

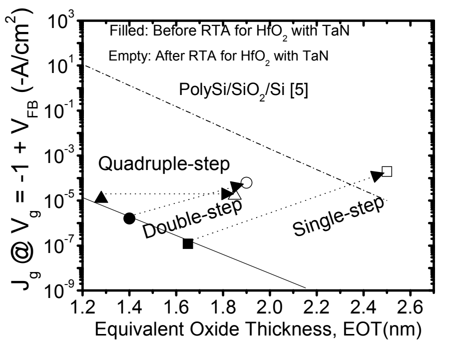

Fig. 8. Multi-step deposited HfO_2 shows smaller increase in EOT and leakage current after high temperature RTA.