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The sheet resistance instability in the sub-100 nm tungsten poly-metal wordline due to an *in-situ* NH₃ pre-annealing during the sealing nitride deposition

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INTRODUCTION

Tungsten-shunted polymetal gate electrode structure, W/WN_x/poly-Si, is an attractive candidate for giga-bit density memory devices in a narrow gate length less than 100 nm, because it shows a lower sheet resistance (Rs) than that of tungsten polycide structure (WSi_x/poly-Si). Although the sheet resistance of polymetal gate electrode is known to be nearly an order lower than that of polycide electrode [1,2], a sealing treatment with a thin nitride film is critically required right after gate reoxidation in order to prevent the W electrode from oxidizing and/or damaging by the subsequent processes. Furthermore, an *in-situ* NH₃ pre-anneal process during nitride deposition has recently been proven to be very efficient in suppressing an abnormal tungsten oxidation (whisker formation), because these whiskers can cause a wordline-to-bitline short [3].

In this article, we demonstrate that the wordline sheet resistance of tungsten polymetal gate electrode could be enormously devastated, as close to a narrow gate length less than 100 nm, when NH₃ anneal time is excessively long. Utilizing physical analyses such as x-ray diffraction (XRD) and secondary ion mass spectroscopy (SIMS), the surface regions of tungsten sidewall have been found to transform into a tungsten nitride (WN) after being excessively annealed in high temperature NH₃ ambient. This surface-localized (<70 nm) WN formation also caused a microscopic sidewall inflation of tungsten electrode, giving rise to a difficulty of gapfilling in between wordlines. Optimizing the annealing time resolves the Rs degradation based on the WN transition without whisker formation.

EXPERIMENTAL

For the purpose of gate length-dependent wordline sheet resistance (Rs) measurement, W(700 Å)/WN_x(50 Å)/n⁺ poly-Si(700 Å)/SiO₂(50 Å)/p-Si nMOS structures with various gate length size were fabricated on the p-type (100) Si substrate. After gate electrode patterning, gate selective reoxidation and diluted H₂SO₄ cleaning were performed in sequence. Then, thin nitride film (~70 Å) was deposited at 710 °C by low-pressure-chemical-vapor-deposition (LPCVD) method. For sealing nitride deposition, an *in-situ* NH₃ pre-anneal process was carried out right before nitride deposition, where NH₃ anneal times were adjusted to find out an optimal condition. Finally, thin silicon dioxide (SiO₂) and nitride films were sequentially deposited as a buffer and a spacer film, respectively. The detailed process sequence is given in Fig. 1. For the material analyses such as XRD and SIMS, same gate stacks were prepared without any patterning and NH₃ pre-anneal nitride film and buffer oxide film deposition were also performed.

RESULTS AND DISCUSSION

Figure 2 shows the wordline Rs with gate length, where the NH₃ pre-anneal time was adjusted. The larger the gate length is, the smaller the impact of the NH₃ pre-anneal time is. At less than sub-100 nm size, three times more Rs increase was

observed at the long time (LT) annealed sample compared to the short time (ST) ones.

Table I displays the Rs values measured on the film stack of the buffer oxide/sealing nitride/W/WN_x/n⁺ poly-Si/SiO₂/p-Si without patterning. Regardless of depositing a buffer oxide, the Rs value in LT samples is ~1.5 times higher than one in ST-2 samples. Although Rs values in ST-2 annealed sample are slightly larger than ones in the control sample (without NH₃ pre-anneal & nitride film deposition), the WO₃ whisker growth can be avoided by employing the ST-2 annealing. As an evidence of whisker formation in the control sample, Fig. 3(a) shows the whisker morphology and a Rs value of tungsten film also slightly increases upon rapid thermal annealing in N₂. Figure 4 shows the XRD results where weak W-N peaks correspond to WN and W₂N. These W-N peaks are observed only in LT samples, not in ST-2 ones. Since the electrical resistivity of W-N films is several times higher than that of pure tungsten film [4], the Rs increase in LT samples should be explained by a WN formation at sidewalls during NH₃ anneal at high temperature. The SIMS depth analyses shown in Fig. 5 also demonstrate that nitrogen profile exponentially decreases from the surface implying the surface-localized tungsten nitride transition. Close to short (<100 nm) gate length, whole tungsten film transforms into tungsten nitride during LT annealing, giving rise to the unexpectedly high Rs in LT samples.

Furthermore, the tungsten nitride transition caused a topological inflation of gate sidewalls, as shown in cross-sectional TEM image [Fig. 6(a)]. Along with tungsten nitride transition, this inflation feature is also based on the increase of average lattice spacing due to nitrogen incorporation into the tungsten film. As shown in Fig. 7, two theta angle of W(110) decreases with the NH₃ pre-anneal time. The sidewall inflation feature makes it difficult to gapfill in between wordlines by interlayer dielectrics, so microscopic voids usually form. To avoid these issues, the *in-situ* NH₃ pre-anneal time should be optimized as evidenced in this work.

CONCLUSION

We found that excessively long-time *in-situ* NH₃ pre-annealing right before sealing nitride deposition could cause the tungsten sidewall nitridation and inflation as closer to the short gate length. This also leads to the abnormal increase of the wordline sheet resistance and makes it difficult to gapfill between gate lines with interlayer dielectrics. Since the control sample without NH₃ pre-annealing grows WO₃ whiskers on the tungsten sidewall, conclusively, an *in-situ* NH₃ pre-anneal time should be minimized within the limit of whisker-free condition.

REFERENCES

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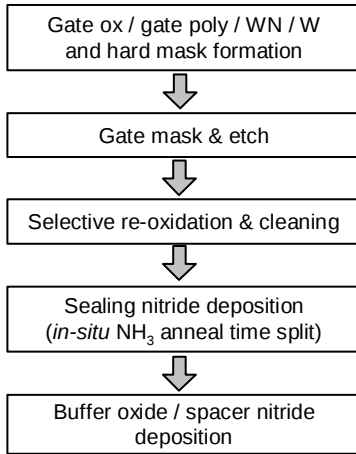


Figure 1. Process sequence.

Table I. Sheet resistances of W(700 Å)/WN_x(50 Å)/n⁺ poly-Si(700 Å)/SiO₂/p-Si stack.

Sample	control	LT		ST-2	
Sealing Nitride (70 Å)	X	in-situ NH3 pre-anneal			
Rs (Ω/sq.)	2.22	3.7	3.77	2.59	2.57
RTA	N2-950 °C-15sec				
Buffer Ox. (80 Å)	X	X	HTO-SiO2	X	HTO-SiO2
Rs (Ω/sq.)	2.27	3.41	3.47	2.43	2.42

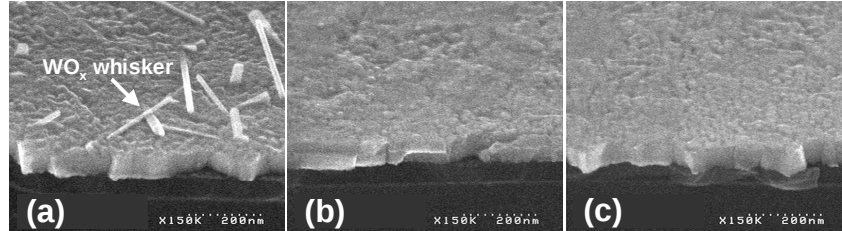


Figure 3. SEM images of tungsten surface after RTA 950 °C-15sec: (a) without sealing nitride over-layer, (b) with sealing nitride layer (LT annealed), and (c) with sealing nitride layer (ST-2 annealed)

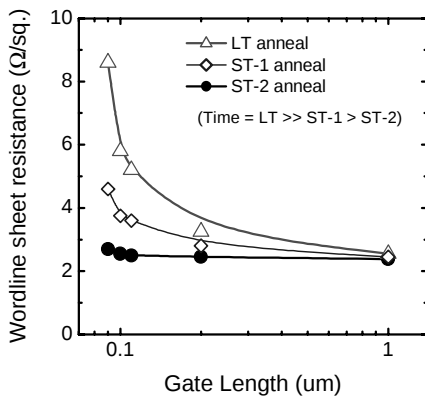


Figure 2. Wordline sheet resistances with the gate length of W/WN_x/n⁺ poly-Si gate.

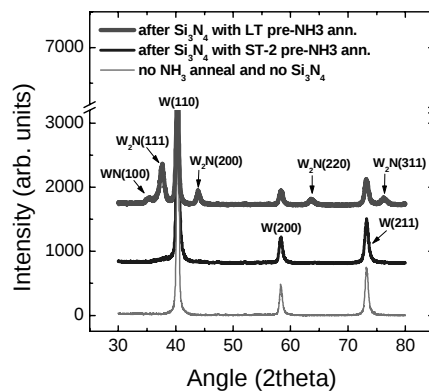


Figure 4. X-ray diffraction data of Si₃N₄(70 Å)/W/WN_x/n⁺ poly-Si/SiO₂/p-Si with various NH₃ pre-anneal times before Si₃N₄ deposition.

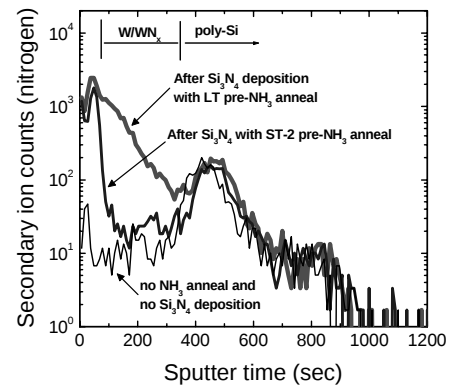


Figure 5. SIMS depth profiles of Si₃N₄(70 Å)/W/WN_x/n⁺ poly-Si/SiO₂/p-Si with NH₃ pre-anneal time splits before Si₃N₄ deposition.

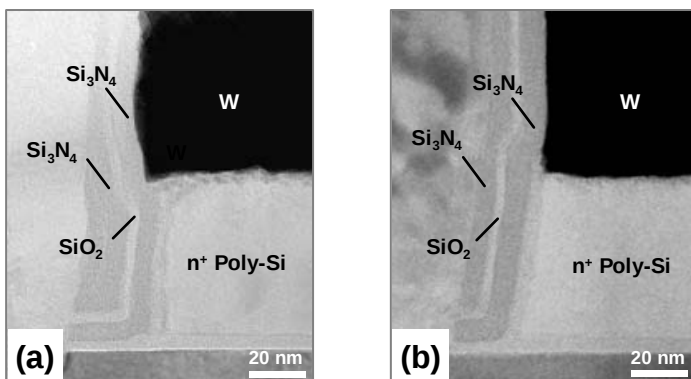


Figure 6. Cross-sectional TEM images of W/WN_x/n⁺ poly-Si/SiO₂/p-Si gate electrode with NH₃ pre-anneal before Si₃N₄ deposition (Si₃N₄/SiO₂/Si₃N₄ spacer scheme adopted): (a) with LT annealed before Si₃N₄ deposition, (b) with ST-2 annealed before Si₃N₄ deposition.

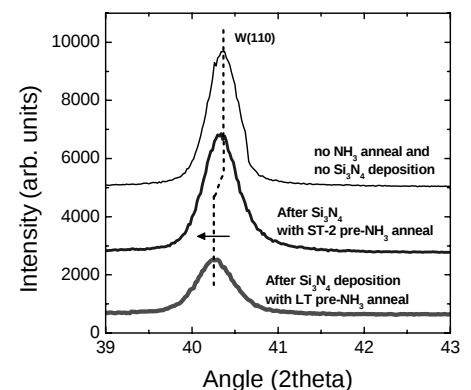


Figure 7. X-ray diffraction spectra of Si₃N₄/W/WN_x/n⁺ poly-Si/SiO₂/p-Si with *in-situ* NH₃ pre-anneal time splits before Si₃N₄ deposition. Spectra nearby W(110) peak are focused.