Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 484-485

P3-18

Influence of interface layers and bottom electrodes on $(Ba,Sr)TiO_3$ thin film leakage current

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1.Introduction

In order to achieve higher performance and lower power dissipation of ultra-large scale integrated circuits, the scaling rule is inevitable as a guiding principle for semiconductor device miniaturization. For capacitor application it is necessary to obtain sufficient capacitance with reduced cell area so that the reduction of dielectric thickness is needed, resulting in the increase of leakage current under a constant electric field. Therefore, high-dielectric constant materials such as $(Ba,Sr)TiO_3$ (BST) [1]must be developed for capacitor applications. In this paper, the influences of interface layers and bottom electrodes between BST and Si are investigated.

2.Experimental

After RCA cleaning, Si(100) substrates were dipped into 0.5 % HF solution. 1 nm thick silicon nitride (SiN) as an interface layer was deposited by either atomic layer deposition (ALD) or thermal nitridation (TN). 20nm thick Ir, Ti, and Ta were deposited independently as a bottom electrode on Si using direct current magnetron sputtering. 100 nm thick BST thin film was deposited on SiN by radio-frequency magnetron sputtering at 50 W at room temperature. The BST thin films were also deposited on the bottom electrode at 450˚C and 50W. Sequential sputtering conditions were controlled as follows; Ar gas introduction (1.5 Pa: 40 sccm) for 1 min, subsequently, oxygen addition (2.0 Pa, $Ar:O_2$=43.6 sccm:10.9 sccm) for 99 min 12 sec. The deposition rate was 0.98 nm/min. Annealing was carried out at 650°C in N_2 ambient. 100 nm thick Ir top electrode was deposited on the BST film using direct current magnetron sputtering with a screen mask of ϕ2 mm at 1.0 Pa in Ar ambient. Aluminum electrode with a thickness of 400 nm was deposited on the backside of silicon at 0.67 Pa in Ar. A sample structure and measurement set-ups for dielectric relaxation are shown in Fig. 1[2].

3.Results and Discussion

Figure 2 shows leakage current versus applied voltage for various interface layers and bottom electrodes between BST and Si. From C-V measurement and TEM, it is found that Ta and Ti layers were oxidized during BST deposition so that Ir/BST/TaO_x/Si and Ir/BST/TiO_x/Si capacitors were formed, respectively. Ir was also oxidized during BST deposition so that Ir/BST/IrO_x/Ir/Si capacitor was formed. Ir/BST/TaO_x/Si capacitor shows the lowest leakage current, while Ir/BST/TiO_x/Si capacitor was the highest.

In order to investigate the leakage current characteristics, influence of measurement time on the leakage current was investigated. Applied voltage form is shown in Fig. 3. The influence of delay time on leakage current of Ir/BST/IrO_x/Ir/Si, Ir/BST/SiO_2/Si, and Ir/BST/TaO_x/Si, capacitors are shown in Figs. 3, 4 and 5, respectively. Ir/BST/SiN(ALD)/Si, Ir/BST/SiN(TN)/Si capacitors were also investigated. Integration time was set at 266 msec. Ir/BST/IrO_x/Ir/Si, Ir/BST/SiO_2/Si, Ir/BST/SiN(ALD)/Si, and Ir/BST/SiN(TN)/Si capacitors show similar characteristics. At low electric field, the leakage current decreased with the delay time. At high electric field, no time dependence was observed. Low electric field regions in which time-dependence was observed for Ir/BST/IrO_x/Ir/Si, Ir/BST/SiO_2/Si, Ir/BST/SiN(ALD)/Si, Ir/BST/SiN(TN)/Si capacitors were between –1 and +3V, -1 and +1V, -4 and +4V, and -4 and +4V, respectively. Leakage current of Ir/BST/TaO_x/Si capacitor did not depend on applied voltage, but decreased with delay time. Similar results were obtained for integration time dependence. Figures 6, 7, and 8 show influence of measurement temperature on leakage current of Ir/BST/IrO_x/Ir/Si, Ir/BST/SiO_2/Si, and Ir/BST/TaO_x/Si capacitors, respectively. Ir/BST/SiN(ALD)/Si, Ir/BST /SiN(TN)/Si capacitors were also investigated. At low electric field, no temperature dependence of leakage current was observed. On the other hand, at high electric field, the leakage current increased with temperature. Ir/BST/IrO_x/Ir/Si, Ir/BST/SiO_2/Si, Ir/BST/SiN(ALD)/Si, and Ir/BST/SiN(TN)/Si capacitors showed similar characteristics. Leakage current of Ir/BST/TaO_x/Si capacitor was independent of temperature. Consequently, the leakage current mechanism of Ir/BST/IrO_x/Ir/Si, Ir/BST/SiO_2/Si, Ir/BST/SiN(ALD)/Si, and Ir/BST /SiN(TN)/Si capacitors at low electric field and Ir/BST/TaO_x/Si capacitor was found to be dielectric relaxation current. Figure 9 shows dielectric relaxation current of Ir/BST/IrO_x/Si Ir/BST/SiO_2/Si, Ir/BST/TaO_x/Si, and Ir/BST/TiO_x/Si capacitors as a function of time. These I-t characteristics can be described using Curie-Von Schweilder relaxation model of

$$J_{DR}(t)=J_0t^{-n} \quad (1)$$

In order to investigate the leakage current mechanism, at higher electric field, Frenkel-Poole plots of capacitors are shown in Fig. 10. Dielectric constants calculated from Frenkel-Poole plots for Ir/BST/IrO_x/Ir/Si and Ir/BST /SiO_2/Si capacitors were 1.94 and 1.3 respectively. On the other hand, dielectric constants calculated from Shottoky plot were less than 1.0. Consequently, the leakage current mechanism of Ir/BST/IrO_x/Ir/Si, Ir/BST/SiO_2/Si capacitors at higher electric field is Frenkel Poole emission.

4.Coclusion

Influence of interface layers and bottom electrodes on $(Ba,Sr)TiO_3$ film leakage current was investigated. Ir/BST/TaO_x/Si capacitor shows the lowest leakage current, while Ir/BST/TiO_x/Si capacitor shows the highest. Leakage current mechanism of Ir/BST/TaO_x/Si capacitor was dominated by dielectric relaxation current because

Frenkel-Poole emission was suppressed. Leakage current mechanism of Ir/BST/IrO_x/Ir/Si, Ir/BST/SiO_2/Si, Ir/BST/SiN(ALD)/Si, and Ir/BST/SiN(TN)/Si capacitors were dielectric relaxation current at low electric field, and Ir/BST/IrO_x/Ir/Si, and Ir/BST/SiO_2/Si capacitors indicated Frenkel-Poole emission at higher electric field.

References

[1] T. Kikkawa, N. Fujiwara, H. Yamada, S. Miyazaki, F. Nishiyama, and M. Hirose, Appl. Phys. Lett. 81, 2821 2002

[2] H. Reisinger, G. Steinlesberger, S. Jakschik, 267 IEDM 2001

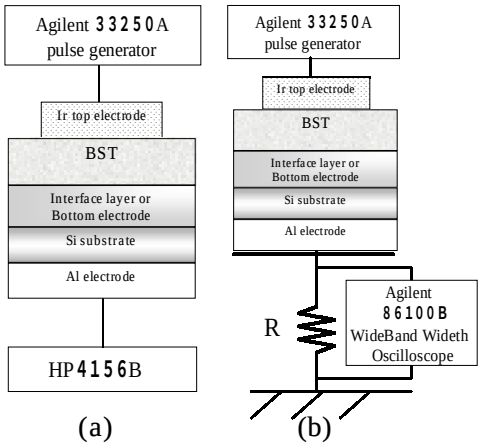

Fig. 1. Sample structures and measurement set-ups
(a) Dielectric relaxation $t>10^{-3}$ sec.
(b) Dielectric relaxation $t<10^{-3}$ sec.

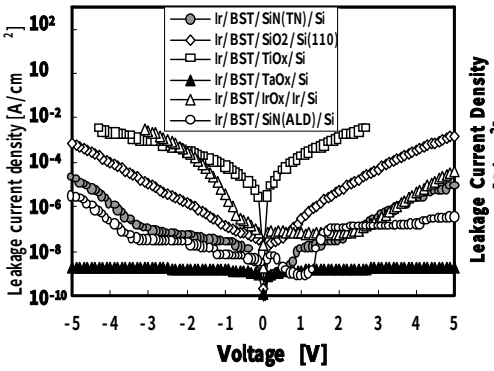

Fig. 2. Leakage current versus voltage for various interface layers and bottom electrodes.

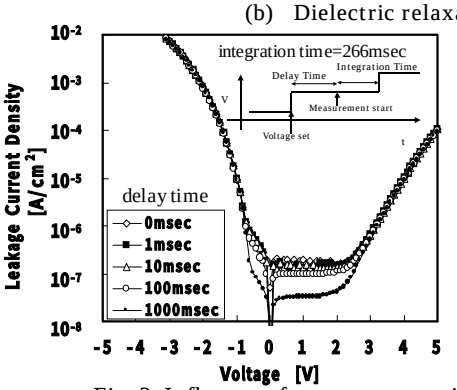

Fig. 3. Influence of measurement time on the leakage current versus voltage for Ir/BST/IrO_x/Ir/Si capacitor.

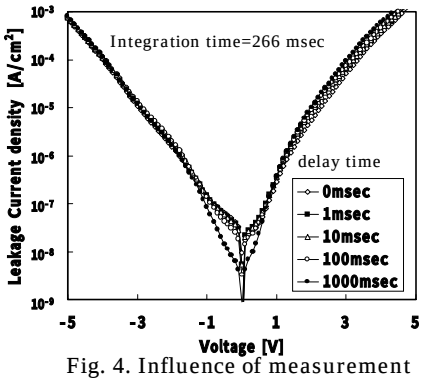

Fig. 4. Influence of measurement time on the leakage current versus voltage for Ir/BST/SiO_2/Si capacitor.

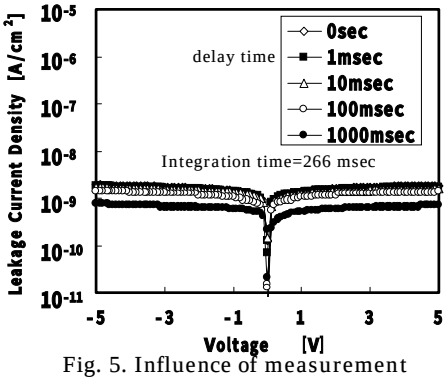

Fig. 5. Influence of measurement time on the leakage current versus voltage for Ir/BST/TaO_x/Si capacitor.

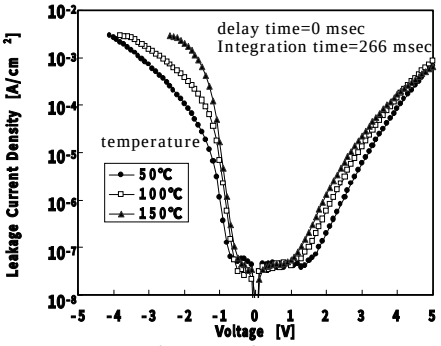

Fig. 6. Influence of measurement temperature on the leakage current versus voltage for Ir/BST/IrO_x/Ir/Si capacitor.

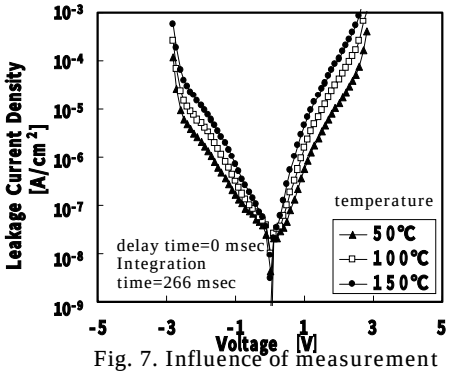

Fig. 7. Influence of measurement temperature on the leakage current versus voltage for Ir/BST/SiO_2/Si capacitor.

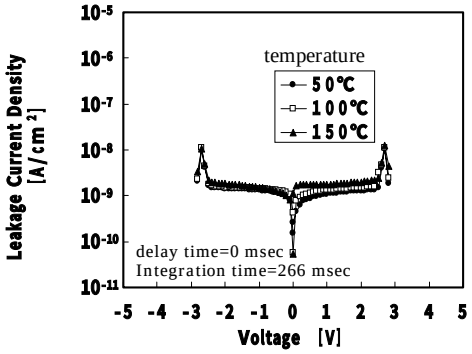

Fig. 8. Influence of measurement temperature on the leakage current versus voltage for Ir/BST/TaO_x/Si capacitor.

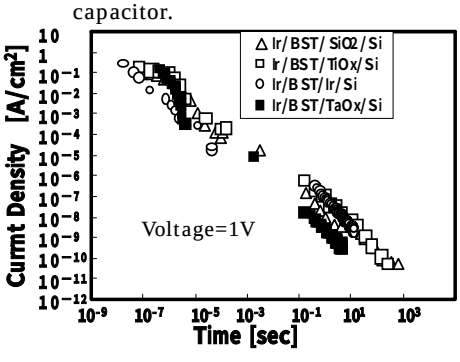

Fig. 9. Dielectric relaxation currents for Ir/BST/SiO_2/Si, Ir/BST/Ti/Si, Ir/BST/IrO_x/Si, and Ir/BST/TaO_x/Si capacitors.

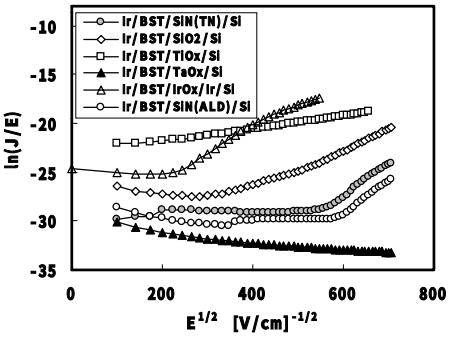

Fig. 10. Frenkel-Poole plots of leakage currents of Ir/BST/IrO_x/Ir/Si, Ir/BST/SiO_2/Si, Ir/BST/TaO_x/Si, Ir/BST/SiN(ALD)/Si, and Ir/BST/SiN(TN)/Si capacitors.