Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 460-461

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An Integrated Gate Stack Process for Sub-90nm CMOS Technology

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Abstract

A high quality ultra-thin plasma nitrided oxide (EOT~12.5Å) is fabricated by the clustering of gate dielectric process in a production-worthy tool. Compared to conventional plasma nitrided oxide process, cluster process shows 1.2 Å reduction in inversion oxide thickness (Tox_inv) due to less moisture induced-oxide re-growth and nitrogen out diffusion. In addition to significant Tox_inv reduction, cluster process offers devices that exhibit better device performance and superior reliability characteristics in terms of SCE, Vt roll-off, DIBL and 2X lifetime improvement in NBTI, thus making it very promising for sub-90nm CMOS.

Introduction

In order to improve the device performance, gate oxide thickness has been scaled aggressively. The gate leakage current increases significantly because direct tunneling becomes the primary conduction mechanism as oxide is scaled down to below 1.5 nm. The high gate leakage current not only degrades device performance due to inversion charge loss, but also increases standby power consumption. One efficient way to reduce leakage current is to use a physically thicker gate dielectric with a high dielectric constant, which provides the same electrically equivalent SiO_2 thickness. Recently, remote plasma nitridation (RPN) and decoupled plasma nitridation (DPN) on SiO_2 have been demonstrated for their gate current reduction [1,2]. In this work we demonstrate, for the first time, a highly reliable production-worthy ultra-thin plasma nitrided oxide (PNO) process utilizing the cluster of base-oxide, plasma nitridation, post-anneal and poly deposition. Experiment results indicate that the clustering of PNO process is very promising for sub-90nm CMOS applications.

Process

CMOS devices were fabricated using state-of-the-art 90nm foundry technology [3]. The main process steps are shown in Fig.1. Shallow trench isolation (STI) was used for isolation followed by retrograde well formation. After channel implantation, PNO process was performed. Different from conventional PNO, cluster PNO integrates base-oxide, plasma nitridation, post-anneal and poly deposition together. After LDD, spacer formation and S/D implantation, RTA was carried out, followed by NiSi salicide formation.

Tox reduction

The cross-sectional TEM of conventional and cluster PNO is shown in Fig. 2. By using cluster process in the load-luck system, about 1.5 Å physical thickness reduction was observed. The plots of Jg vs. Tox_inv show consistent results with TEM in Fig. 3. The Tox_inv reduction in PFET is smaller than NFET due to poly depletion effect. In Fig. 4, it shows that the nitrogen peak at Si/SiO_2 interface of cluster PNO is higher than the conventional one. The schematic in Fig. 5 illustrates the mechanisms of thinner PNO oxide produced by cluster process. In conventional approach, base-oxide, plasma nitridation, post-anneal and poly deposition steps are processed in their individual tool. Thus, the occurrence of nitrogen out-diffusion and oxide re-growth caused by moisture between these steps is adverse to EOT scaling in PNO process.

Performance and reliability

Fig. 6 depicts the NFET Vt roll-off characteristics of conventional and cluster PNO. Devices with cluster PNO show less Vt roll-off and drain-induced-barrier- lowering in spite of less reverse short channel effect. In Fig 7, no obvious Vt shift was observed in PFET between cluster and conventional PNO. This implies the N out-diffusion is mostly occurred at the top surface of oxide. Fig 8 shows the normalized Gm of PFET versus the vertical electrical field. In the low field region, normalized Gm of cluster PNO is slightly degraded as compared to the conventional one. However, in the high field region, two splits are merged. Similar results are observed in NFET as shown in Fig. 8. Fig. 9 shows the intrinsic TDDB of conventional and cluster PNO. Although the Tox_inv of cluster oxide is thinner than conventional one by 1.2 Å, the oxide lifetime data show comparable results. Since the NBTI is very sensitive to nitrogen concentration at the Si/SiO_2 interface, NBTI lifetime of the two approaches is examined as shown in Fig. 10. Results indicate cluster PNO have 2X improvement in NBTI resistance than conventional one at a given field. This is probably due to its sharper nitrogen profile in oxide region and better Si/SiO_2 interface quality.

Conclusions

We have demonstrated a high performance and high reliable cluster PNO oxide. The cluster PNO and device shows better EOT scalability, excellent SCE Vt roll-off, comparable TDDB and better NBTI as compared to conventional PNO process.

Acknowledgements

We would like to express sincere thanks to coworkers in TSMC R&D and QRA for their discussion and support.

References

[1] C.H. Chen *et al.*, *EDL*, p.260, 2001.
[2] H. H. Tseng *et al.*, *EDL*, p.704, 2002.
[3] *C.C. Wu et al., IEDM,p.65, 2002.*

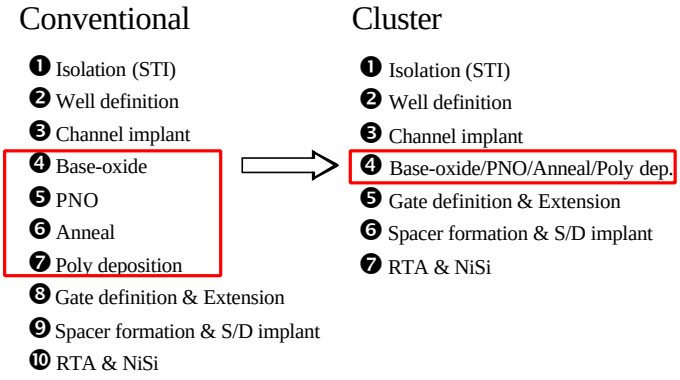

Fig 1. Key process steps of device fabrication..

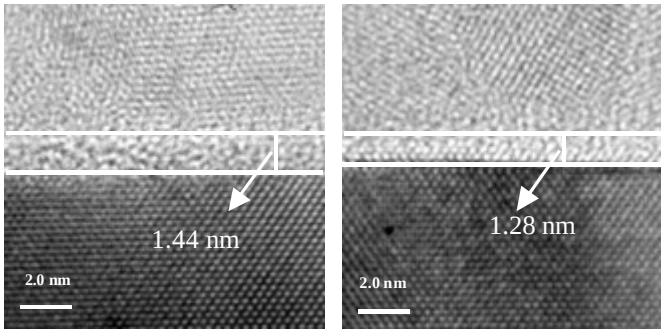

Fig. 2. Cross-section HRTEM of conventional and cluster PNO.

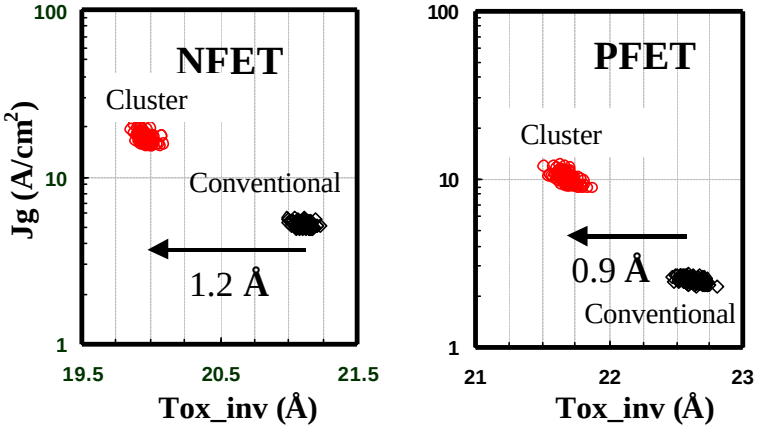

Fig 3. Jg vs. Tox_inv for NFET and PFET devices with conventional and cluster PNO process.

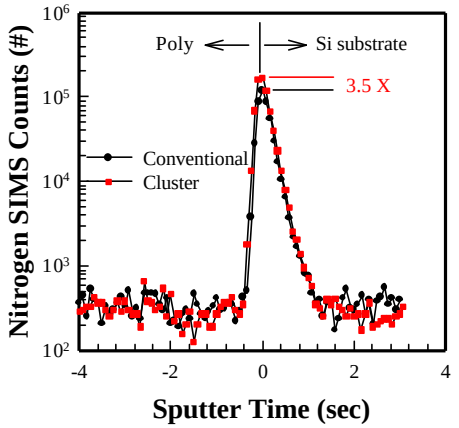

Fig 4. Nitrogen SIMS counts at Si/SiO_2 interface after fully process.

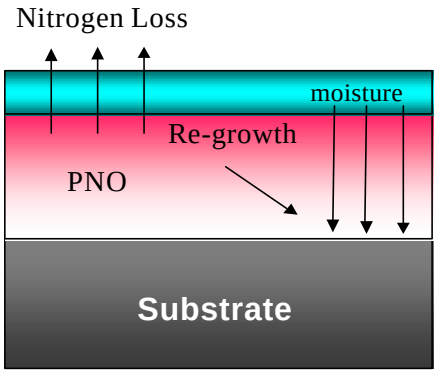

Fig. 5. Mechanism of thinner PNO oxide produced by cluster process.

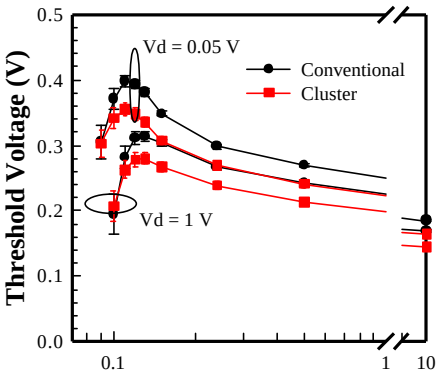

Fig. 6. Threshold voltage roll-off of n-channel MOSFET.

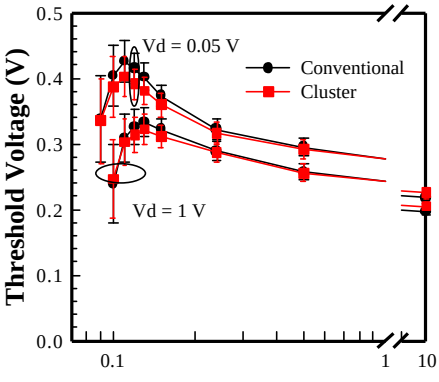

Fig. 7. Threshold voltage roll-off of p-channel MOSFET.

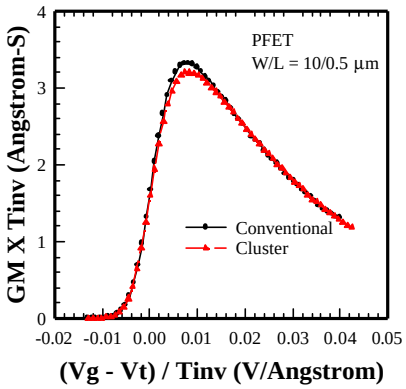

Fig. 8. Normalized Gm between conventional and cluster PNO oxide.

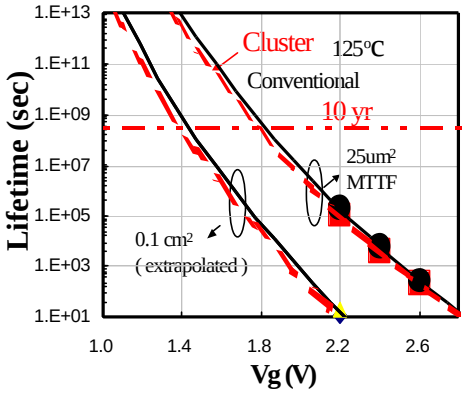

Fig. 9. Intrinsic TDDB for conventional and cluster PNO oxide.

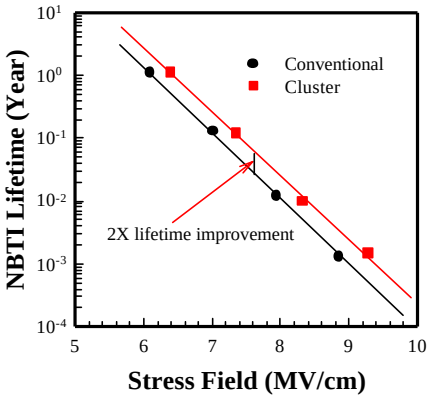

Fig. 10. NBTI lifetime of conventional and cluster PNO oxide.