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Improving the Accuracy of Modified Shift-and-Ratio Channel Length Extraction Method Using Scanning Capacitance Microscopy

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1. Introduction

As MOSFETs are scaled down to 100 nm, it is increasingly challenging to extract the effective channel length, L_{eff} accurately. Various kinds of methods have been explored to extract the electrical L_{eff}. However, some methods exhibit certain limitations that yield unreasonably high values of L_{eff} as MOSFETs are scaled down while others are difficult to implement in routine electrical testing of deep-submicron MOSFETs in the industry. We have previously proposed a modified Shift-and Ratio (MS&R) method [1] by which it is simpler and easier to generate L_{eff} than original shift-and-ratio method [2]. The values of L_{eff} generated by MS&R method are more reasonable than the original shift-and-ratio method with much less computation time involved thus much more convenient for routine electrical testing of deep-submicron MOSFETs in the industry. Recently, direct channel length measurement using Scanning Capacitance Microscopy (SCM) [3, 4] have been shown to give good results. Although SCM measurement is affected by other experimental parameters, such as tip convolution, surface oxide quality and sample preparation, it is uniquely able to provide direct physical imaging of MOSFET structure. In this context, SCM measurement can be used as a complimentary tool to improve the accuracy of electrical L_{eff} extraction method. We have studied the cross-sections of the MOSFETs using SCM and by comparing our extracted L_{eff} measurement with that of the SCM measurement, we are able to show the consistency of our L_{eff} extraction method. In addition, SCM measurement is used as a control to generate a correction factor (*CF*) to further improve the accuracy of our modified Shift-and Ratio method.

2. Modified Shift-and-Ratio method

The MOSFETs under study were fabricated using 0.13 µm and 0.1 µm CMOS technology on 200 mm Si wafers as reported in paper [1]. The source and substrate voltage of the MOSFETs were grounded (V_s=V_b=0). The drain voltage (V_d) set to 0.05 V. The gate voltage (V_g) was swept from 0 V to 1 V in the steps of 0.001 V. The drain current (I_d) was then measured to obtain the current-voltage (IV) curve for L_{eff} extraction.

The measurement was carried out at a gate voltage range close to threshold voltage. Within this range, we can fairly assume that the mobilities of short channel transistor and long channel transistor are similar. Thus, a more rational L_{eff} can be extracted even with halo implant. Next, in order to examine the effect of different gate voltage ranged at low bias with respect to the accuracy of extracted L_{eff}, three different V_{gs} were applied to extracted the L_{eff} These three ranges were 0.1 V to 0.5 V, 0.1 V to 0.4 V and 0.1 V to 0.3 V. The effective channel lengths extracted from n-channel NMOS transistors with L_{drawn} of 0.12µm, 0.13µm and 0.15µm for different V_{gs} ranges were shown in Fig. 1.

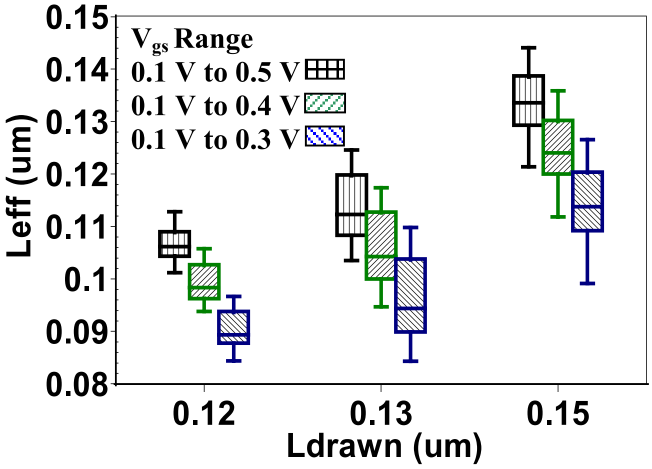

Fig. 1 L_{eff} extracted for different *Vgs* range for 0.13µm technology NMOS transistors. V_{ds} was bias at 0.05V.

Fig. 1 shows that the extracted L_{eff} was smaller as the V_{gs} ranges decreased. Similar trend was observed for both NMOS and PMOS transistors for both 0.13 µm technology and 0.1 µm technology. The effective channel length extracted in the *Vgs* range of 0.1 V to 0.3 V was fairly constant with $\Delta L = L_{drawn} - L_{eff}$, around 0.032 µm for NMOS and around 0.051 µm for PMOS for the 0.13 µm technology. For 0.1 µm technology, ΔL calculated is around 0.018 µm for NMOS and around 0.033 µm for PMOS.

3. SCM Measurement

Fig. 2 shows the SCM image of the cross-sectioned PMOS transistor. From the SCM image, channel length, L_{SCM}, of the MOSFET can be obtained by measuring the distance between two source/drain (S/D) extension. To minimize the tip convolution effect, a transmission electron microscope (TEM) was used to calibrate the results obtained by SCM. The SCM measurements for both NMOS and PMOS transistors are shown in Tables I and II respectively.

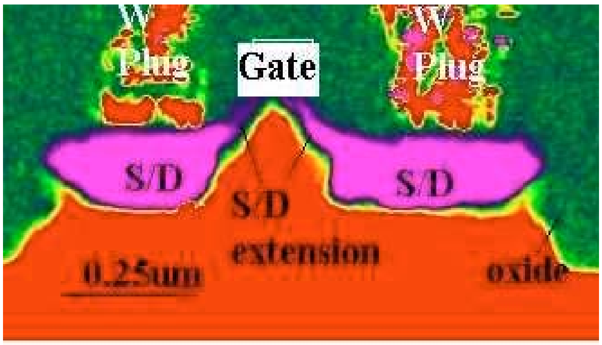

Fig. 2. Scanning capacitance microscopy images of the PMOS transistor.

4. Results and Discussion

Table I shows the effective channel length extracted by the modified Shift and Ratio method, original Shift-and-Ratio method and channel length measurement by SCM for NMOS transistors for both technologies. Both MS&R and SCM measurement generate consistent results, $L_{gate} - L_{SCM}$ is around 0.025 μm. L_{gate} is the physical gate length measured by XTEM for 0.1μm technology with $L_{gate} - L_{SCM}$ around 0.035 μm for 0.13 μm technology. $L_{gate} - L_{ef}$ is around 0.012μm and 0.018 μm for 0.1μm and 0.13μm technology respectively. PMOS transistor measurements are shown in Table II, $L_{gate} - L_{SCM}$ is approximately 0.043 μm and 0.046 μm for 0.1μm and 0.13 μm technology respectively. $L_{gate} - L_{ef}$ is around 0.027μm and 0.035 μm for 0.1μm and 0.13μm technology respectively. With this information, a correction factor CF can be calculated. $CF = L_{SCM} / L_{eff}$ can be used to improve the accuracy of our modified Shift-and-Ratio method. Tables I and II show that the L_{eff} generated by the original Shift-and-Ratio method has been over-estimated.

5. Conclusion

We have successfully used a modified Shift-and-Ratio method to extracted the L_{eff} for devices fabricated by state-of-the-art CMOS technology. In addition, we have studied the cross-sectioned of very short channel MOSFET using SCM. Comparing the L_{eff} extracted using modified Shift-and-Ratio method, original S&R method and L_{SCM} measured using SCM, all three measurements show the consistency with respect to $L_{gate.}$ However, MS&R method yields a L_{eff} nearer to SCM measurement than original Shift-and-Ratio method. In addition, MS&R method is non-destructive and can be routinely used on full-wafer measurement. Since SCM is able to provide direct physical imaging of MOSFET, it can be used as a verification tool for MS&R method. To improve the accuracy of MS&R, a correction factor (CF) was generated by using the channel length value extracted from SCM.

References

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Table I: Comparisons of extracted L_{eff} values for NMOS transistors among MS&R,S&R, and SCM measurement with different L_{drawn} for both 0.13 μm and 0.1 μm technology. L_{gate} is the physical gate length measured by XTEM

L_{drawn} (μm)	L_{gate} (μm)	L_{SCM} (μm)	$L_{gate} - L_{SCM}$ (μm)	MS&R L_{eff} (μm)	S&R L_{eff} (μm)	L_{gate} – MS&R L_{eff} (μm)	$CF = L_{SCM}$ / MS&R L_{eff}
0.08	0.075	0.052	0.023	0.063	0.109	0.012	0.8254
0.09	0.085	0.059	0.026	0.072	0.117	0.013	0.8194
0.12	0.105	0.071	0.034	0.09	0.143	0.015	0.7889
0.13	0.115	0.08	0.035	0.096	0.149	0.019	0.8333

Table II: Comparisons of extracted L_{eff} values for PMOS transistors MS&R, S&R and SCM measurement with different L_{drawn} for both 0.13 μm and 0.1 μm technology. L_{gate} is the physical gate length measured by XTEM.

L_{drawn} (μm)	L_{gate} (μm)	L_{SCM} (μm)	$L_{gate} - L_{SCM}$ (μm)	MS&R L_{eff} (μm)	S&R L_{eff} (μm)	L_{gate} – MS&R L_{eff} (μm)	$CF = L_{SCM}$ / MS&R L_{eff}
0.08	0.075	0.0311	0.044	0.048	0.121	0.027	0.6479
0.09	0.085	0.0426	0.042	0.057	0.126	0.028	0.7474
0.12	0.105	NA*	NA*	0.067	0.123	0.038	NA*
0.13	0.115	0.069	0.046	0.081	0.131	0.034	0.8519

* Not Available