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Effect of Vacuum Annealing on High-k Dy_2O_3 Thin Films Deposited on Si(100)

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1. Introduction

High-k gate insulator is the key technology to suppress the gate leakage current in sub 100 nm CMOS with SiO_2 gate insulators. ZrO_2, HfO_2 and their aluminates and/or silicates so far have been the most promising, however, these materials still have some problems such as interfacial layer with lower dielectric constant during the post deposition annealing process that led to the increase of EOT. Rare earth oxides are also the candidate materials for alternative SiO_2 gate insulator, and excellent results for La_2O_3, Pr_2O_3, Gd_2O_3 etc. have been reported so far. Recently, it was reported that the formation of interfacial layer during the post deposition annealing process was able to be suppressed by annealing under low oxygen partial pressure such as 10^{-7} Torr [1].

In this paper, the effect of annealing under ultra high vacuum (10^{-9} Torr) was investigated for Dy_2O_3 rare earth oxide thin films deposited on Si(100) [2].

2. Experimental Procedure

Dy_2O_3 thin films (3 – 12 nm) were deposited on HF-last or chemically oxidized Si (100) substrates by e-beam deposition method under ultra high vacuum using oxide targets. H_2O_2 were used to form the chemical oxide layer (0.5 nm) on Si substrates. The deposition temperature was room temperature (RT) - 400°C. The pressure in the chamber during depositions was 10^{-9}~10^{-7} Torr. The deposited film was annealed in the deposition chamber (10^{-9} Torr) at 400˚C for 90 min. Finally, Al electrode (ϕ100 μm) was deposited. For comparison, conventional rapid thermal annealing (RTA) was also carried out in O_2 ambient for 5 min. C-V, I-V, AFM and XPS measurements were performed to characterize the fabricated MIS diodes [3].

3. Experimental Results

Figure 1 shows C-V for 5.5 nm-thick Dy_2O_3 deposited on HF-last Si(100) at RT, followed by the 200 – 1000°C RTA in O_2. The hysteresis in the C-V for the as-deposited film was improved by the RTA, however, the equivalent oxide thickness (EOT) increased with the RTA temperature even by 400˚C RTA. Figure 2 shows the C-V for 4.5 nm-thick Dy_2O_3 *in-situ* vacuum annealed at 400˚C. EOT of 1.1 nm was obtained for as-deposited film and the increase of EOT was found to be suppressed by the *in-situ* vacuum annealing although the significant negative flat-band voltage shift was observed (ΔV_{FB}: -0.96 V). Figure 3 shows the comparison of the leakage current (@V_{FB}+1.5 V) as a function of EOT for Dy_2O_3 films annealed by conventional O_2 RTA and *in-situ* vacuum annealing both at 400˚C. *In-situ* vacuum annealing was found to improve the leakage characteristics without increasing the EOT.

EOT plotted against the physical thickness of the films (T_{phy}) as measured by ellipsometry is shown in Fig. 4. From the slope of this result, the relative dielectric constant

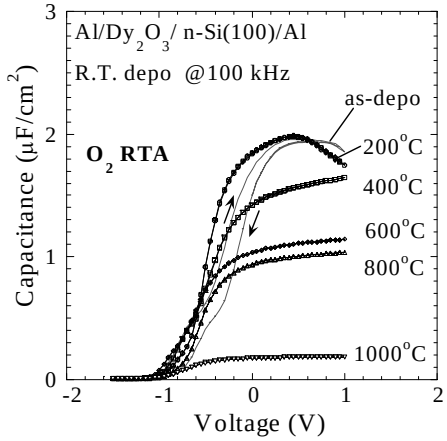

Fig. 1 C-V for 5.5 nm-thick Dy_2O_3 deposited on Si(100). RTA was carried out in O_2 at 200 - 1000˚C for 5 min.

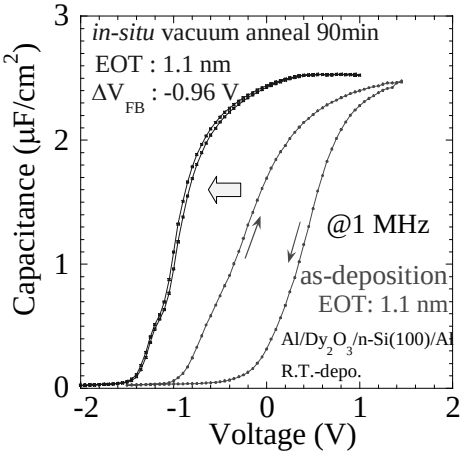

Fig. 2 C-V for 4.5 nm-thick Dy_2O_3 deposited on Si(100) followed by the *in-situ* vacuum annealing at 400˚C for 90 min.

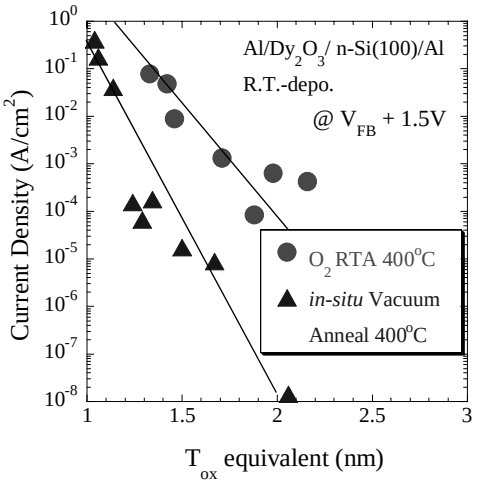

Fig. 3 Comparison of leakage current density for Dy_2O_3 films annealed by conventional O_2 RTA and in-situ vacuum annealing.

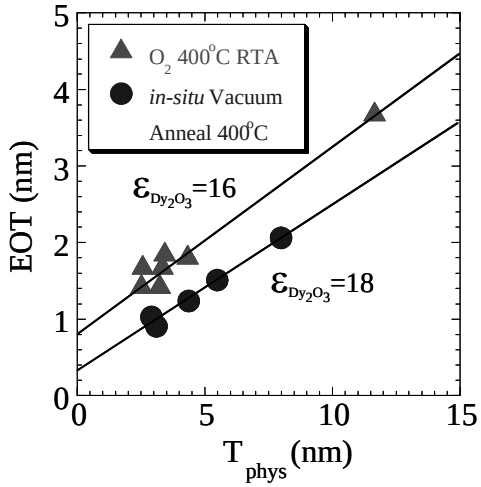

Fig. 4 Plots of EOT vs. T_{phy} for a set of Dy_2O_3 films annealed by conventional O_2 RTA and in-situ vacuum annealing.

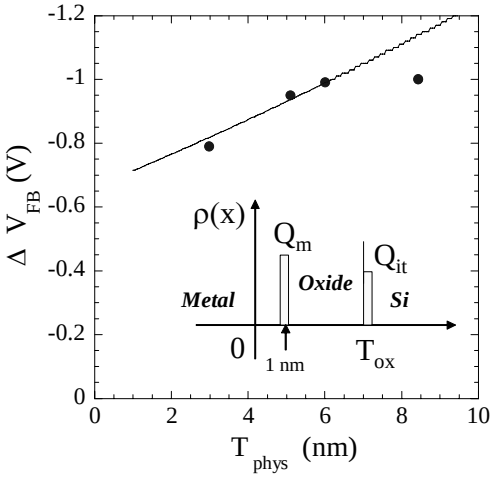

Fig. 5 ΔV_{FB} vs. $T_{phy.}$ and fixed charge distribution model.

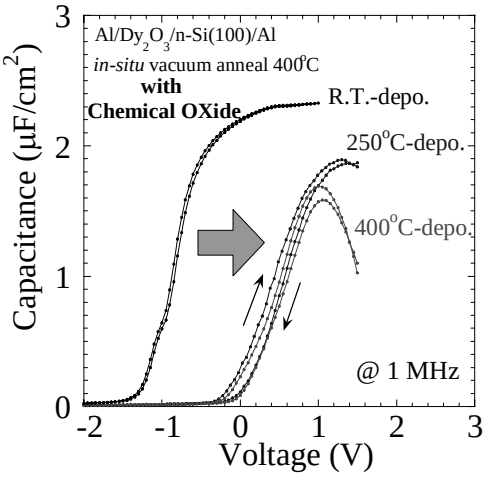

Fig. 6 C-V dependence on the deposition temperature.

was estimated to be approximately 16 for the film annealed by O_2 RTA, while it was 18 for the film annealed by *in-situ* vacuum annealing method. The extrapolated intercept on the ordinate at T_{phy}=0 indicates the presence of an interfacial layer with the equivalent electrical thickness of 0.8 nm for O_2 RTA, while it was 0.4 nm for *in-situ* vacuum annealing, which was thinner than compared to the film annealed by O_2 RTA. The difference of interfacial layer formation was also confirmed by the Si2p XPS measurements (not shown).

Figure 5 shows fitting results of the fixed charge distribution estimated from the results of V_{FB} shifts in C-V, and it was found to be fitted well when the fixed charge located both at Dy_2O_3/Si and Metal/Dy_2O_3 interfaces as shown in the inset of figure. Therefore, the interface should be improved prior to the annealing process. In order to improve the Dy_2O_3/Si interface properties, Dy_2O_3 films were deposited on the chemically oxidized Si substrates with increasing the deposition temperature. As shown in Fig. 6, the negative V_{FB} shifts were found to be suppressed by increasing the deposition temperature to 250 or 400˚C, and better C-V characteristic was obtained by 250˚C deposition (ΔV_{FB}=0.08 V).

4. Conclusions

Ultra-high vacuum annealing was investigated for Dy_2O_3 deposited on Si(100). The leakage current was decreased without increasing of EOT by vacuum annealing method. Negative V_{FB} shift was suppressed by increasing the deposition temperature of Dy_2O_3 from RT to 250˚C.

Acknowledgements

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