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Impact of Ti/TiN (Glue/Barrier Layer) Formation on Ultra-thin Gate Oxide Reliability (HCI and NBTI) for Deep Sub-micron CMOS Transistors

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1. Introduction

Use of a low temperature Ti/TiN (glue/barrier) layer is essential in producing deep sub-micron CMOS transistors with high performance and excellent reliability. TiN has been widely used in the IC industry as a diffusion barrier and adhesion layer material for tungsten (W) and aluminum (Al) interconnects. Because the step coverage and conformality of TiN becomes increasingly important as device dimensions shrink, CVD TiN is preferred compared to PVD TiN. In general, the CVD TiN process has been developed to achieve high step coverage, low resistivity, and low defect density. CVD TiN can be deposited using $TiCl_4$ and NH_3[1]:

$$6TiCl_4 + 8NH_3 \Rightarrow 6TiN + 24HCl + N_2, \quad (1)$$

in which the deposition temperature ranges from 450 to 750°C. It should be noted that chlorine (Cl) is always incorporated in the TiN film through this $TiCl_4$-based CVD process and the amount increases as the deposition temperature decreases, which may increase the resistivity. However, it will be shown that an appropriate amount of Cl introduced by this process can improve HCI and NBTI reliability. The TiN film can also be deposited by means of metal organic precursors [2]. One popular example is to thermally deposit TiN from TDMAT, i.e. $Ti[N(CH_3)_2]_4$, carried by helium (He) carrier gas:

$$Ti[N(CH_3)_2]_4 \Rightarrow TiN(C,H) + HN(CH_3)_2 + \text{other hydrocarbons}, \quad (2)$$

where the deposition temperature is 400 to 500 °C. In this MOCVD TiN process, hydrogen and carbon impurities are contained in the film, which can be reduced by a subsequent in-situ N_2-H_2 plasma treatment.

Although TiN is an excellent diffusion barrier material, TiN directly in contact with silicon results in a high contact resistance. A Ti layer below the TiN is usually utilized as a glue layer to ensure good contact resistance [3]. The Ti layer can be formed by ion metal plasma (IMP) PVD technique [4]. In brief, IMP Ti process is to ionize the sputtered atoms from the Ti target and then deposit the sputtered atoms. The Ti layer can also be deposited by $TiCl_4$-based PE (plasma enhanced) CVD process [5] as follows:

$$TiCl_4 + 2H_2 + 2Si \Rightarrow TiSi_2 + 4HCl, \quad (3)$$

in which the deposition temperature ranges from 400 to 700°C.

In this work, we investigate the impact of different Ti/TiN deposition processes on HCI and NBTI reliability, and it's found that IMP Ti / $TiCl_4$-based CVD TiN layer exhibits low contact resistance and excellent HCI & NBTI reliability.

2. Experimental

All the devices used in this study were simultaneously processed using a standard CMOS fabrication technique as briefly summarized in Fig. 1, in which different Ti/TiN deposition methods were processed as listed in Table I. A HP4284 LCR meter in parallel mode was used for capacitance-voltage (C-V) measurement, and a HP4156 semiconductor parameter analyzer was utilized for the measurement of electrical properties and reliability characteristics.

3. Results and Discussions

Figure 2 and Fig. 3, respectively, show the Ion-Ioff characteristics and gate to inversion channel C-V characteristics of (a) nMOSFETs and (b) pMOSFETs for different deposition methods of the Ti/TiN layer. It is apparent that the Ion-Ioff characteristics or C-V characteristics is independent of Ti/TiN formation technique. On the other hand, the contact resistance of N-poly and P-poly is shown in Fig. 4, in which condition B ($TiCl_4$-based CVD Ti/TiN) and condition D (IMP Ti/ $TiCl_4$-based CVD TiN) demonstrate lower contact resistivity. The higher contact resistivity for condition A (IMP Ti/MOCVD TiN) and condition C ($TiCl_4$-based CVD Ti/MOCVD TiN) can be explained by the organic material impurities in the film as indicated in (2).

Figure 5 shows the hot carrier degradation for nMOSFETs at the maximum substrate current (Isub,max) stress condition. It is clear that condition A has the worst hot carrier immunity, and condition D exhibits slightly better hot carrier reliability characteristics than condition B and C.

Figure 6 compares the threshold voltage shift versus stress time for pMOSFETs during a typical NBTI stress [6] at a stress bias of –2.6V and an elevated temperature of 150 °C. As seen in Fig. 6, condition D has the best NBTI immunity. It should be mentioned here that Fig. 5 and 6 represent the typical HCI and NBTI reliability characteristics for twelve samples tested.

4. The Effect of Chlorine

Among four different formation methods, the glue/barrier layer formed by IMP Ti/ $TiCl_4$-based CVD TiN demonstrates the best HCI and NBTI reliability for the first time. A model has been proposed to explain the phenomena as follows. Some of the chlorine contained in the TiN film formed by $TiCl_4$-based CVD process diffuses to gate dielectrics through IMP Ti film (columnar structure) and poly-Si gate. The presence of chlorine in the gate dielectrics can passivate dangling bonds in the gate oxide transition region by forming Si-Cl bonds, and accordingly improve HCI and NBTI reliability because Si-Cl bonds are more difficult to break than Si-H bonds under HCI or NBTI stress.

Acknowledgment

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Table I: Ti/TiN (glue/barrier layer) formation methods.

Conditions	A		B		C		D	
glue/barrier layer	Ti	TiN	Ti	TiN	Ti	TiN	Ti	TiN
MOCVD		X				X		
IMP	X						X	
TiCl4-based CVD			X	X	X			X

- STI
- Well and channel implantation
- Dual gate oxynitride (2.6 & 6.5nm)
- Gate poly-Si deposition
- Offset spacer formation
- Extension implantation
- SiN sidewall spacer deposition
- S/D implantation and activation
- Co salicide formation
- Metallization

Fig. 1 CMOS fabrication process flow.

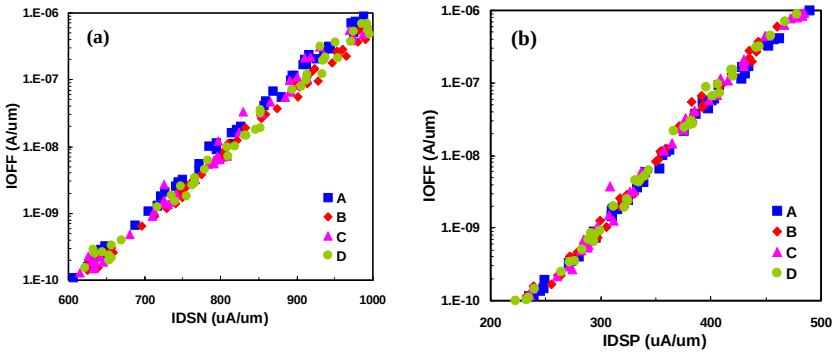

Fig. 2 Ion versus Ioff characteristics of (a) nMOSFETs and (b) pMOSFETs for different deposition methods of the Ti/TiN layer.

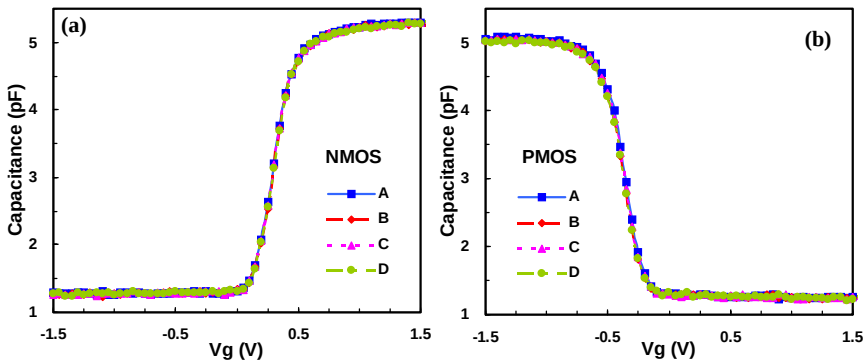

Fig. 3 C-V characteristics of (a) nMOSFETs and (b) pMOSFETs for different deposition methods of the Ti/TiN layer.

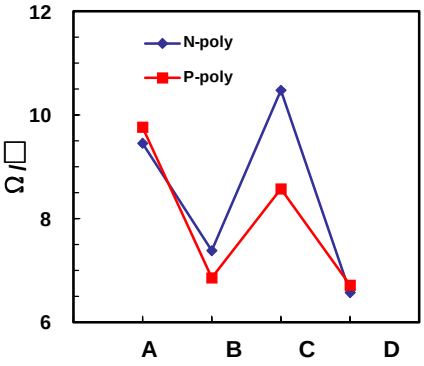

Fig. 4 Contact resistance of N-poly and P-poly for four Ti/TiN formation methods as listed in Table I.

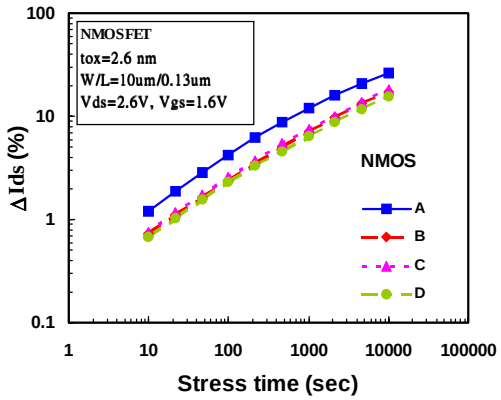

Fig. 5 Hot carrier injection (HCI) degradation for nMOSFETs at maximum substrate current stress condition.

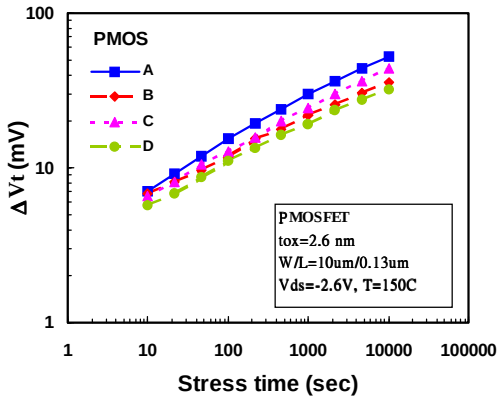

Fig. 6 Threshold voltage shift versus stress time under negative bias temperature instability (NBTI) stress.