Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 520-521

P4-15

Characterization and Comparison of Strained $Si_{1-y}C_y$ MOSFET Grown by Gas Source MBE and Hot Wire Cell Method

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1. Introduction

Recently, group IV alloys such as $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ have attracted great attention as new materials for introducing band gap engineering in the present Si technology. Furthermore, the challenge of improving device performance is carried out by the enhancement of transport properties in a MOS channel using strained $Si/Si_{1-x}Ge_x$ structure. However, it is difficult to prepare the buffer layer with a high crystal quality and a flat interface for this strain system. We focused on the strained $Si_{1-y}C_y/Si$ structure since it has several advantages, compared to using $Si_{1-x}Ge_x$. It is a simple structure without a relaxed buffer layer. Furthermore, the thermal conductivity of $Si_{1-x}Ge_x$ is inferior to that of Si.

Previously, we succeeded to grow the strained $Si_{1-y}C_y$ films with a substitutional carbon content up to 1 at. % by using gas-source (GS) MBE and hot-wire CVD. In this work, we applied these films to MOSFET and investigate the electrical characteristics of strained $Si_{1-y}C_y$ layer.

2. Experimental results and discussion

The epitaxial $Si_{1-y}C_y$ layers were grown by GS-MBE and Hot Wire (HW) Cell method. For GS-MBE, Si_2H_6 and C_2H_2 were used as source gases and the substrate temperature was 600°C. For HW-Cell method, SiH_4 and C_2H_2 were used and the substrate temperature was 200°C. The details of each growth conditions were shown in references [1,2]. For the fabrication of MOSFET, source and drain regions were firstly fabricated by thermal diffusion at 900°C prior to the growth of strained $Si_{1-y}C_y$ films, in order to avoid thermal damage to the films. Then the $Si_{1-y}C_y$ films were grown at the gate region as a channel, using each method. The thickness of the films was about 50 nm. The films grown by HW-Cell at a low temperature were annealed at 800°C for 30 minutes for a desorption of hydrogen. The gate oxide was grown by wet oxidation for 10 minutes at 800°C and its thickness was 20 nm. The gate length was 5 μm and width was 20 μm.

Figure 1 shows the dependence of normalized effective electron mobility on substitutional carbon contents (C_s). The carbon contents were varied up to 1 at. %, which is

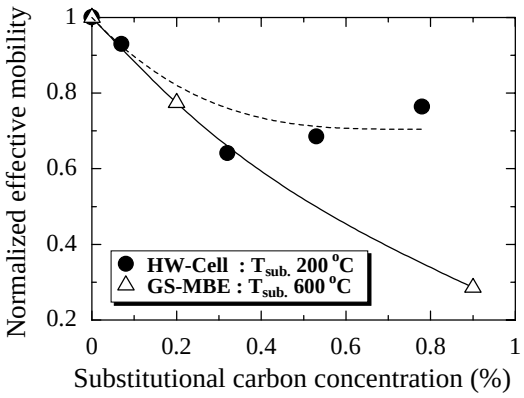

Figure 1. Dependence of normalized effective electron mobility on substitutional carbon contents.

sufficient for the improvement in electron mobility according to our calculation results. However, the effective mobility of $Si_{1-y}C_y$ MOSFET was decreased by increasing carbon content. It decreased by 20% for the MOSFET (C_s=0.8%) fabricated by HW-Cell method at a low temperature of 200°C while it decreased by 70% for MOSFET (C_s=0.9%) fabricated by GS-MBE at 600°C.

The reasons for the decrease in electron mobility were (1) alloy scattering caused by substitutional carbon, and (2) scattering caused by interstitial carbon. The roughness of $SiO_2/Si_{1-y}C_y$ interface might be affect the mobility in this system, however it was comparable between these two, fabricated by HW and GS-MBE. To analyze these results, we studied carrier transport properties in strained $Si_{1-y}C_y$ layer by Monte Carlo method. For the calculation of scattering rate, Fermi's golden rule was used and three scattering mechanisms were considered: acoustic phonon, intervalley f- and g-type optical phonon scattering, and alloy scattering. The band split in conduction band caused by strained was assumed as 65meV per 1 at.% of carbon. For the calculation of alloy scattering, the rate W(k) was given by following equation [3].

$$W(k) = \frac{3\pi^3}{8\hbar} V_0 U^2_{alloy}\, x(1-x) N(E_k) \qquad (1)$$

V_0 is a volume of the primitive cell, U_{alloy} is random alloy potential, x is alloy mole fraction, and $N(E_k)$ is

density of states. Alloy potential (U_{alloy}) is unknown parameter so that we varied from 0eV to 2.0eV. We also assumed that other physical parameters of the $Si_{1-y}C_y$ were the same as Si, because the carbon content is small. The temperature was 300K. Figure 2 shows the dependence of normalized calculated electron mobility on carbon content and U_{alloy}. The electron mobility would increase by adding carbon even though the U_{alloy} is 1.0eV. However it would merely decrease when the U_{alloy} is larger than 1.5eV. The decrease of electron mobility was about 15% with 1 at.% of C_s, assuming the U_{alloy} was 2.0eV. Since the U_{alloy} is usually a difference of electron affinity between two materials, that is 0.55eV for Si and 3C-SiC, it is considered that the alloy scattering is not the only factor which decrease the electron mobility by 70% in the $Si_{1-y}C_y$ films grown by GS-MBE.

Then we focused on the interstitial carbon in the $Si_{1-y}C_y$ films and its relation with the growth temperature. In figure 2, the difference of amount of decrease in effective electron mobility between MOSFET fabricated by HW-Cell and GS-MBE would be considered as due to the difference in substrate temperature. Figures 3 and 4 show the dependence of XRD pattern of the $Si_{1-y}C_y$ films grown by GS-MBE and by HW-Cell, respectively, on substrate temperature. The flow rate ratios of C_2H_2/Si_2H_6 and C_2H_2/SiH_4, respectively, were the same at each temperature. The peak of $Si_{1-y}C_y$ films grown at high temperature shifted to lower angle by increasing substrate temperature, indicating the larger amount of interstitial carbon exists in the films. On the other hand, the peak position didn't change for the films grown by HW at a low temperature of around 200°C. According to the model suggested by Osten et. al [4], when the substrate temperature was high, the Si adatom which arrived at the surface would kick out the carbon atom out of lattice position, forming a Si-C interstitial complex or the C-C dimers on the surface. This result indicated that lowering growth temperature would restrict the increase of interstitial carbon and cause the improvement of electrical characteristics of $Si_{1-y}C_y$ films. It well agreed with our experimental results shown in figure 2.

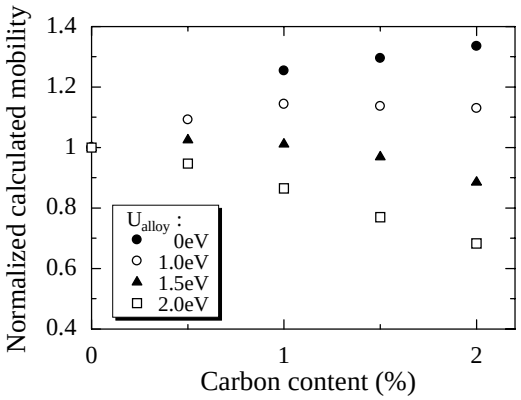

Figure 3. Dependence of normalized calculated electron mobility on carbon content as a function of alloy potential.

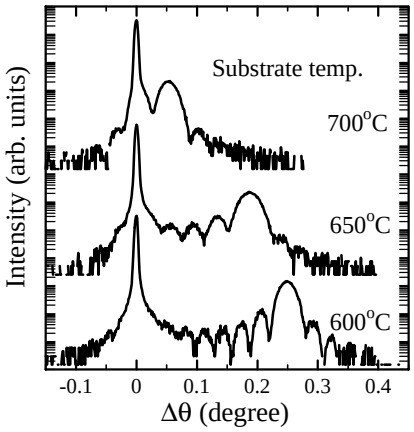

Figure 3. Dependence of XRD pattern of the $Si_{1-y}C_y$ films on substrate temperature by using GS-MBE

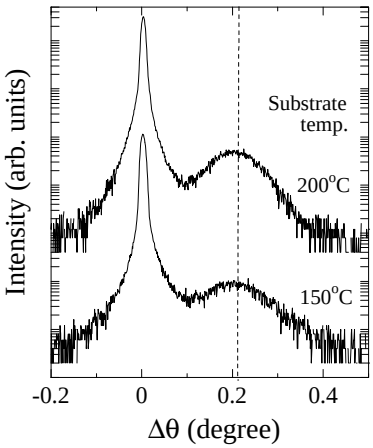

Figure 4. Dependence of XRD pattern of the $Si_{1-y}C_y$ films on substrate temperature by using HW-Cell method

3. Conclusion

$Si_{1-y}C_y$ MOSFET was fabricated by GS-MBE and HW-Cell method and their electrical characteristics were compared. The electron mobility of MOSFET fabricated by GS-MBE showed large decrease while that fabricated by HW-Cell method showed slight decrease. This difference was due to the difference in interstitial carbon concentration, suggesting the lowering growth temperature would improve the electrical characteristics of $Si_{1-y}C_y$ films.

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