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Electrical properties and conduction mechanism of ZrO_2 films on $Si_{1-y}C_y$

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1. Introduction

Fundamental limits to CMOS scaling are rapidly approaching as devices are scaled below the 50 nm ranges. New methods and materials for CMOS fabrication must be investigated to allow continued device improvement. The ITRS 2002 update [1] proposes an aggressive requirement for equivalent physical oxide thickness of 1-1.4 nm (it was 1-1.6 nm) by 2007. Gate leakage reduction in ultrathin gate dielectrics is the main motivation for the search of high-k dielectrics [2]. ZrO_2 is being considered as potential candidate for the replacement of SiO_2 due to its high dielectric constant (ε = 20) and low leakage current. $Si_{1-y}C_y$/Si heterolayers are being considered for high temperature applications. Due to its high in-plane mobility, it is also attractive for high performance MOS devices.

In this paper, we present the results of our study on the electrical properties of ZrO_2 thin films deposited on strained $Si_{1-y}C_y$ heterolayers at a low temperature (150°C) using microwave PECVD. We demonstrate the feasibility of integration of high-k ZrO_2 gate dielectric with the strained $Si_{1-y}C_y$ for the first time.

2. Experimental

ZrO_2 films (140 Å) were deposited using metallorganic compound [ZTB, $Zr(OC(CH_3)_3)_4$] in a microwave (700 W, 2.45 GHz) PECVD system at 150°C on solid phase epitaxially grown $Si_{1-y}C_y$ layer [3]. The capacitance-voltage (C-V), conductance-voltage (G-V) and current-voltage (I-V) characteristics were measured using MIS capacitors with an Al gate (area: 1.96×10^{-3} cm^2).

3. Results and Discussions

Fig. 1 shows the Zr 3d XPS spectra of the as-deposited ZrO_2 films. The Zr 3d spectrum shows two peaks (deconvoluted) at 183.1 and 185.8 eV binding energy and are both characteristic of fully oxidized Zr.

Fig. 2 shows the C-V and G-V characteristics of the ZrO_2 gate oxides measured at different frequencies in the range of 20 kHz to 100 kHz. A frequency dependence of the flatband voltage is observed; which is attributed to the presence of interface traps. The maximum value of the conductance increases with increasing frequency because of oxide capacitance in series with the interface trap resistance-capacitance network [4]. The fixed insulator charge density and interface trap density were found to be 2.6×10^{11} cm^{-2} and 5.6×10^{11} $cm^{-2}eV^{-1}$ using C-V and G-V characteristics.

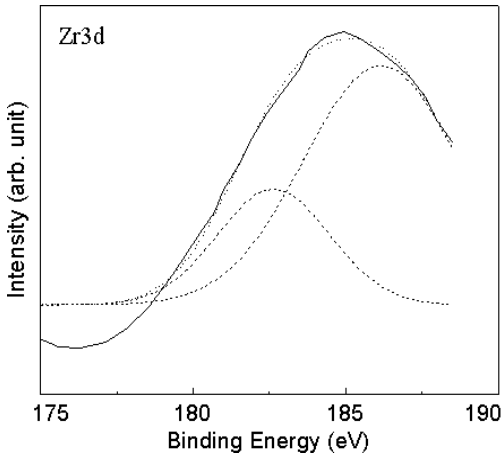

Fig. 1 Deconvoluted Zr 3d spectra for the as-deposited ZrO_2 films on strained $Si_{1-y}C_y$ layers.

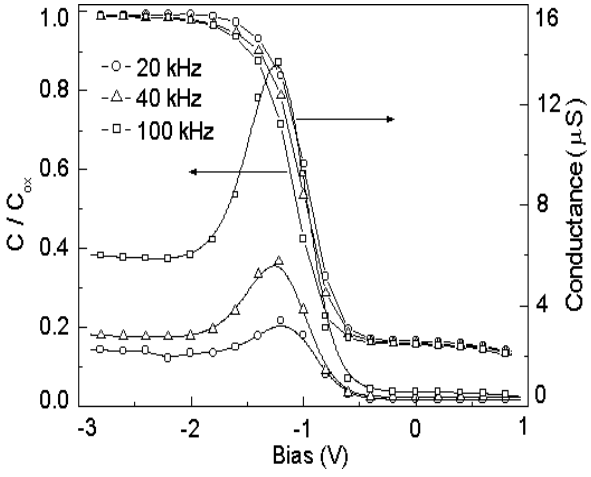

Fig. 2 Frequency dispersion in C-V and G-V characteristics.

In order to study the temperature dependence of interface states in detail, C-V and I-V characteristics were measured at several temperatures in the range of 25-200°C and are shown in Figs. 3 and 4. Fig. 3 shows that the flatband voltage (V_{FB}) follows closely the temperature dependence of the work function difference between Al and strained $Si_{1-y}C_y$. The $\ln(I/T^2)$ vs $E^{1/2}$ plot of ZrO_2 films show a linear relationship and the conduction mechanism is dominated by the Schottky emission [4] as shown in Fig. 5.

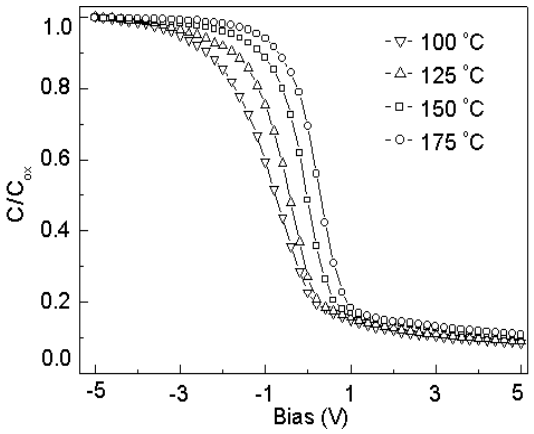

Fig. 3 C–V characteristics of ZrO_2 films.

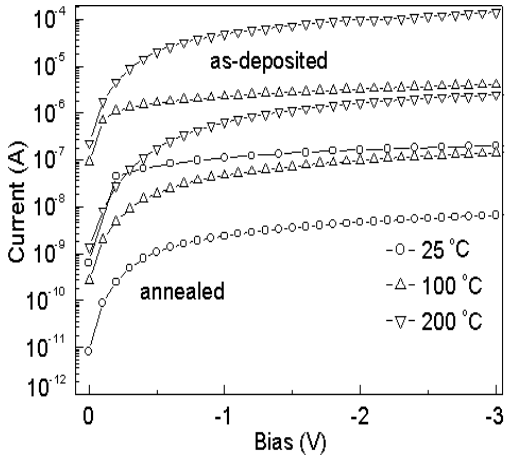

Fig. 4 I-V characteristics of of ZrO_2 films .

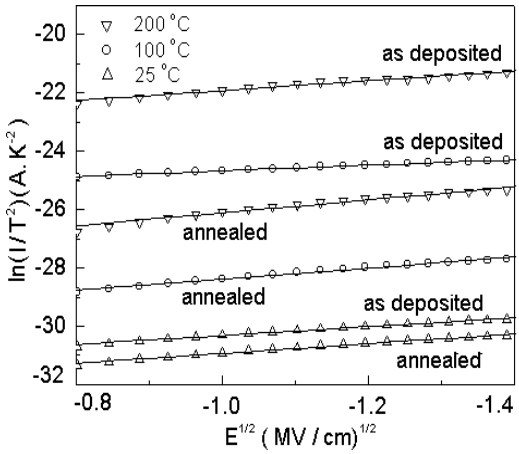

Fig. 5 The $\ln(I/T^2)$ vs $E^{1/2}$ plot for as-deposited and annealed ZrO_2 films at different temperature.

The leakage current is weakly temperature dependent in the low gate voltage region (< - 0.6 V), while the current increases sharply with temperature at higher gate bias. From Fig. 6, it is observed that the data approximately follows a straight line, indicating that gate leakage current varies exponentially with 1/T. The temperature dependence of leakage current is low in samples annealed at 400°C compared to as-deposited ZrO_2 films. These results suggest that the trap-assisted contribution of the gate current is much reduced after N_2 anneal.

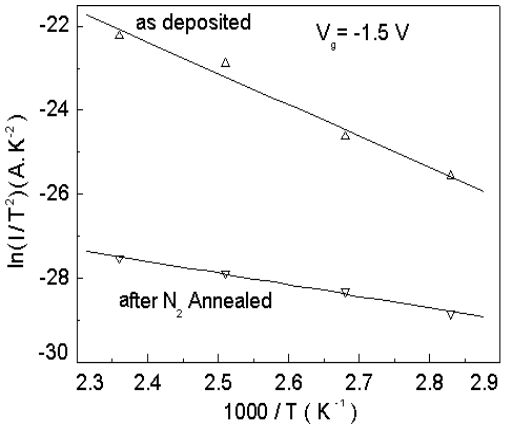

Fig. 6 The $\ln(I/T^2)$ vs 1000/T plot for as-deposited and annealed ZrO_2 films.

4. Conclusion

The electrical properties of low temperature (150°C) plasma deposited ZrO_2 gate oxides on strained-$Si_{1-y}C_y$ are reported. It has been observed that the gate leakage current is reduced after annealing in N_2 ambient, suggesting that the anneal is very effective in reducing the density of traps in the deposited ZrO_2 films. From the temperature dependence of the current-voltage characteristics of the ZrO_2 gate dielectrics, it has been observed that the conduction mechanism is mainly due to Schottky emission at low electric field. Integration of strained-$Si_{1-y}C_y$ and ZrO_2 high-k gate dielectric is demonstrated.

References

[1] International Technology Roadmap for Semiconductors, *Semiconductor Industry Association,* December 2002

[2] C. K. Maiti, S. Chatterjee, G. K. Dalapati, and S. K. Samanta, Electron. Lett. 39, 497, (2003)

[3] S. K. Ray, D. W. McNeill, D. L. Gay, C. K. Maiti, G. A. Armstrong, B. M. Armstrong and H. S. Gamble, Thin Solid Films, 294, 149, (1997)

[4] S. M. Sze, *Physics of Semiconductor Devices Wiley, New York , 2nd Edition*, 362 (1981).