Compact Electrical Characterization of Nano-CMOS Transistor with 1.2nm Ultrathin Gate Dielectric

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Introduction

Aggressive scaling of CMOS devices into nm regime requires ultrathin gate dielectric [1]. The quantum effect entailed therein necessitates the reexamination of the inversion charge [2-5]. Also large gate leakage due to direct tunneling has caused drastic modification of the capacitance-voltage (C-V) behavior. Thus it has become difficult to extract the electrical gate dielectric thickness, threshold voltage and mobility. We extract in this paper the electrical thickness of the gate dielectric from the C-V data and discuss the C-V degradation in terms of the gate leakage (I_G) and channel resistance. We further correlate the C-V with I-V behavior and quantify the inversion charge. The sub-linear increase of the inversion charge with gate voltage is taken into account by introducing the threshold voltage creep (V_{TH}-creep) in the drift-diffusion (DD) I-V modeling. Additionally, the effective mobility (μ_{eff}) and the external resistance have been accurately extracted.

Device Fabrication, Measurement, and Simulation

Fabrication process flow of the nano-CMOS device is shown in Fig. 1. Thin gate dielectric is formed by heavily nitrided plasma oxide [1]. The extension and halo implantations are optimized to minimize the short channel effect and maximize the transistor performance. Thin nickle self-aligned silicide process is also applied. The 50nm gate length NMOS with the thin gate dielectric of 1.35 nm physical thickness is shown in Fig. 2. CV characteristics shown in Fig. 3 is measured at 1MHz. Simulation has been carried out by solving the Shroedinger and Poisson equations self-consistently [2].

Capacitance – Voltage Characteristics

Figure 4 shows the transmission line equivalent circuit of MOS transistor [3]. The intrinsic capacitance (C_i) consists of the poly depletion (Poly), gate dielectric (OX), and Si-substrate (S) capacitance in series. G_i is the effective tunneling conductance. The R_S , R_D , R_B , and R_{Ch} are the series resistance of source, drain, body, and channel, respectively. In order to extract electrical gate dielectric thickness, the parameters such as C_i , G_i , R_S , R_D , R_B , and R_{Ch} should be accurately modeled, measured and simulated. Also shown is our suggested new equivalent circuit for the C_i, in which the quantum effect enters primarily via the inversion capacitance, C_{INV} [2]. Figure 5 shows the simulated C_{INV} , in which the solid lines represent numerical results for classical and quantum theories, respectively. Based on the one-subband triangular potential well approximation, we find that the CINV is divided into two components, i.e. the energy-level-charging capacitance(CE) and the spatial distribution capacitance (C_{AV}) in series. Classically C_{AV} is large, and C_{INV} is practically identical to the conduction band charging capacitance and corresponds to quantum C_E . Quantum mechanically, C_{AV} is comparable to C_E and renders C_{INV} smaller than the classical case. Figure 6 shows channel resistivity (ρ_{CH}) vs. gate voltage (V_G) for the gate lengths of 1.0, 0.5, and 0.1 μ m, respectively. R_T is total resistance defined by V_{DS}/I_{DS} . ρ_{CH} simply extracted by the equation in Fig. 6 decrease drastically with V_G in subthreshold regions, and becomes constant in strong inversion. Once $\rho_{C\!H}$ is known, the external resistance (R_{EXT}) is extracted by subtracting R_{Ch} from the measured R_T (Fig. 7). R_{EXT} is composed of R_S , R_D , and R_{SB} , with R_{SB} indicating the series resistance across the source-tobody junction. For low V_G less than 0.8V, R_{SB} is dominant due to the high source-to-channel barrier. For higher V_G , R_{SB}

vanishes, and $R_{\rm EXT}$ consisting of the usual $R_{\rm S}$ and $R_{\rm D}$ becomes constant. The simulated voltage partition in the MOS capacitor is shown in Fig. 8. The solid and dashed lines represent the voltage partition in the presence and absence of the gate leakage current, respectively. Note that V_R represents the voltage drop induced by R_{Ch} and R_{EXT} coupled with the high I_G . Thus the C-V degradation is easily understood from the decrease of $V_{\rm OX}$ due to the high gate leakage current. Figure 9 shows the C-V data measured from the MOSFET together with the simulation results. The average channel and poly-gate doping extracted from the CV data are &1017 cm-3, 2×1020 cm-3, respectively. The equivalent oxide thickness (EOT) found from the fit to the C-V data is 1.2nm. R_{Ch} (symbols) obtained from the fit to the C-V data is shown in the inset, together with the results from the FV data (line) for comparison. Close agreement between them renders credence to our extraction procedure. The simulated results for channel lengths of 50, 10, 5, and 1 µm MOSFETs show the trend of C-V with channel length reduction [3-5]. The gate leakage does not cause appreciable C-V degradation for the gate length less than $1\mu m$.

Threshold Voltage Creep and Mobility

Figure 10 shows the measured drain conductance (g_D) vs. drain voltage (symbols) and the fits (lines) to the linear g_D . V_{TH} is to be extracted from the intercept on horizontal axis for given V_{G} . V_{TH} thus found is plotted in Fig. 11 where the filled circle denotes the onset V_{TH} of 0.165 V found from the conventional linear extrapolation (LE) method. Indeed, V_{TH} is shown to increase with V_G and the creep effect is shown comparable with the onset value itself for typical V_G range. This creep effect is firmly rooted in the well known sublinear increase of the 2dimensional inversion charge with V_G. Also shown in the inset is the inversion charge $(\boldsymbol{Q}_{\text{INV}})$ extracted classically and quantum mechanically for comparison. Finally μ_{eff} which is inversely proportional to $(V_G - V_{TH})$ can also be accurately extracted by incorporating the creep effect, as shown in Fig. 12. Also shown for comparison is μ_{eff} resulting from the constant V_{TH} and the consistency of introducing the creep effect in the DD I-V model becomes self-explanatory from μ_{eff} – V_G curves.

Conclusions

Compact electrical characterizations of nano-CMOS transistor with 1.2nm ultrathin gate dielectric have been performed for determining the electrical gate dielectric thickness, threshold voltage, and mobility. The observed C-V degradation has been analyzed in terms of gate leakage coupled with R_{EXT} and R_{CH}. It is shown a signature of the gate losing control of the channel inversion. In fact, $R_{\rm EXT}$ and $R_{\rm CH}$ coupled with the gate leakage could constitute a limiting factor for further CMOS device scaling. Inversion capacitance is composed of energy level charging capacitance and spatial distribution capacitance. Finally the sub-linear increase of the inversion charge with V_G is to be incorporated in the drift diffusion I-V model via V_{TH}creep and the effect also enables accurate and consistent extraction of the effective mobility.

References

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- Shallow trench isolation
- Stripping native oxide
- Pretreatment for thin gate oxide
- · Growth of base oxide
- Post Anneal (N2, O2)
- · Poly-Si deposition and patterning
- Extension and halo implantation
- Spike annealing (1100°C)
- Co SALICIDE
- Metallization

Fig. 1 Process flow of CMOS devices with heavily plasma nitrided oxide.



Fig. 2 TEM images of 50 nm NMOS transistor with physical 1.35 nm thin gate dielectric.

100

Classical C





(1.0µm – 0.5µm) ---(1.0μm - 0.1μm)

(0.5µm - 0.1µm)

2



Fig. 4 Typical equivalent transmission line model (left) and our new equivalent circuit (right) of intrinsic capacitance (C_i) and inversion capacitance (C_{INV}) for simulation.



Fig. 7 Measured total resistance $(R_T = V_{DS}/I_{DS})$ and extracted external resistance (\dot{R}_{EXT}) with gate voltage from the channel resistivity (ρ_{Ch}).



Fig. 10 NMOS dain conductance vs. drain voltage. Symbols are data, and lines are fit results to the linear parts.









40m\

1

0.5

DS

Resistivity (

 10^{2}

2

 \dot{C}_{AV} Ċ_E

1/C_E+1/C_{AV})-1

Quantum C_{INV}



Fig. 9 Measured C-V data on $50{\times}50\mu m^2$ NMOSFET at the frequency 1MHz and simulation results with the channel lengths.



Fig. 11 The extracted V_{TH}-creep vs. gate voltage. Inset is extracted inversion charge with and without V_{TH}-creep.



Fig. 12 Extracted effective mobility vs. gate voltage with and without V_{TH} -creep.