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Cross-Hatch Related Oxidation and Reliability of Gate Oxide of Strained-Si/SiGe

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1. Introduction

Strained-Si MOSFETs have attracted much attention because of the improved mobility and current drive capability.[1,2] The 4.2% lattice mismatch between Si and Ge gives rise to strained-Si when epitaxially grown on relaxed SiGe. One of the key considerations in fabricating strained-Si devices is oxidation. It has been reported that oxidation of SiGe shows completely different kinetics from that of Si due to the presence of Ge.[3] The other factor is the role of cross-hatching, the roughness inherent in SiGe material due to the stress fields associated with the underlying misfit dislocations generated during relaxation of the alloy layer. The cross-hatch has been found to cause the interface roughness when the surface of strained-Si layer is oxidized.

In this work, we report that the cross-hatch affects oxidation kinetics not only of the strained-Si surface but also of the SiGe alloy layer under the strained-Si. On the other hand, it is found that reliability of gate oxide does not change or is even improved.

2. Experimental

The strained-Si samples used in this study was grown by CVD process. A 2 μm-thick graded SiGe layer was first grown on Si (100) followed by the growth of 1 μm-thick $Si_{0.7}Ge_{0.3}$ layer and the growth of 20 nm-thick strained-Si layer. MOS capacitors were fabricated on the strained-Si wafer. After RCA cleaning, thermal oxidation was performed at 800°C in pure O_2 ambient. Then, Al gate electrode was formed on the top of oxide layer by vacuum evaporation. In order to avoid degradation due to thermal effects and plasma charging damage, no electrical isolation process was applied and wet chemical etching was used. After SiO_2 on the back side was removed, substrate Au electrode was deposited using vacuum evaporation. For comparison, conventional Si MOS capacitors were also fabricated.

3. Results

Oxidation of strained-Si: AFM images of as-grown strained-Si wafer surface and the wafer oxidized for 1 hour at 800°C (oxide thickness is about 5 nm) are shown in Figures 1(a) and 1(b), respectively. RMS roughnesses were 3.466 and 4.838 nm and the values of the peak-to-valley were 23 and 33 nm in 10 μm $\times$10 μm scan areas, respectively. Figure 2 shows the histogram of roughness for initial strained-Si and oxidized strained-Si surface which clearly indicates the increase in roughness after oxidation. The AFM images shown in Fig. 1 indicate that the roughness increases through non-uniform oxidation along the cross-hatch period as suggested by previous literature.[4]

Oxidation of SiGe: The cross-hatch has been found to affect also the oxidation kinetics of SiGe under the strained-Si layer, when, in particular, the fast-diffusing oxidant such as wet-O_2 is used. Figure 3(a) shows the cross-section of the strained-Si/SiGe oxidized at 850°C for 5 hours in wet-O_2. We can see that oxide grown is not uniform. We also find the formation of a layer in which Ge was condensed up to about 90%. In Figs. 3(b) and 3(c), Fourier transformed patterns of the surface morphology of the as-grown wafer and the oxidized wafer are respectively shown. These indicate that the non-uniform oxidation is associated with the cross-hatch. The results suggest that effects of strain field on diffusion of Si and Ge have to be taken into account for describing oxidation kinetics of strained-Si/SiGe.

Gate Oxide Reliability: Figure 4 shows high frequency C-V characteristics of the strained-Si and bulk-Si MOS capacitors. A plateau exists between gate biases of -1.5 and -2.5 V shows hole confinement in the SiGe beneath the strained-Si layer.

Figures 5(a) and 5(b) show the I-V characteristics of strained-Si and bulk-Si MOS capacitor measured in the accumulation condition. The onset of Fowler-Nordheim tunneling appears at $\sim$-2 and -4 V for strained-Si and bulk-Si, respectively. For strained-Si samples the leakage currents at low biases are smaller than bulk-Si samples. A small current peak at low voltage is observed for bulk-Si samples, which is attributed to condition through the neutral trap distributed in the oxide. This current peak is absent from the characteristic of the strained-Si samples.

Figures 6 shows the Weibull plots of breakdown voltage of samples oxidized at 800°C for 1 hour. When the positive biases were applied, the breakdown voltage slightly decreased. In contrast, a significant improvement in the oxide reliability was observed for strained-Si samples when the negative bias was applied. Since the strained-Si surface is deeply accumulated at the breakdown field as shown in Fig. 4, the improvement is not due to the presence of the Si/SiGe hetero interface but the band alignment at SiO_2/strained-Si and the oxide quality could be of concern.

4. Conclusion

Oxidizing the surface of strained-Si layer and strained-Si/SiGe at relatively low temperature results in increase of surface roughness through non-uniform oxidation along the cross-hatch period. Gate oxide reliability, however, does not change or even improved as compared with an oxide on bulk-Si grown at the same temperature. Investigation on effects of these characteristics on MOSFET performance is in progress.

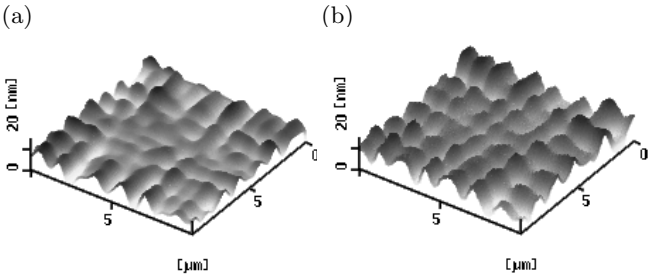

Fig. 1: AFM images taken from strained-Si wafer. (a) before (b) after oxidation for 1 hour at 800°C.

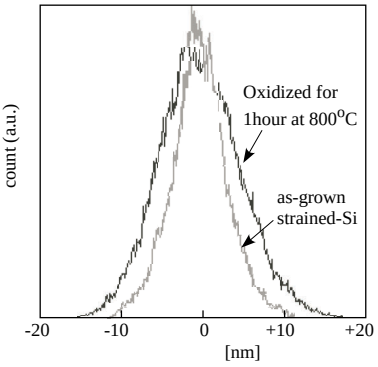

Fig. 2: Histogram of surface roughness for strained-Si (gray line), and oxidized strained-Si (black line).

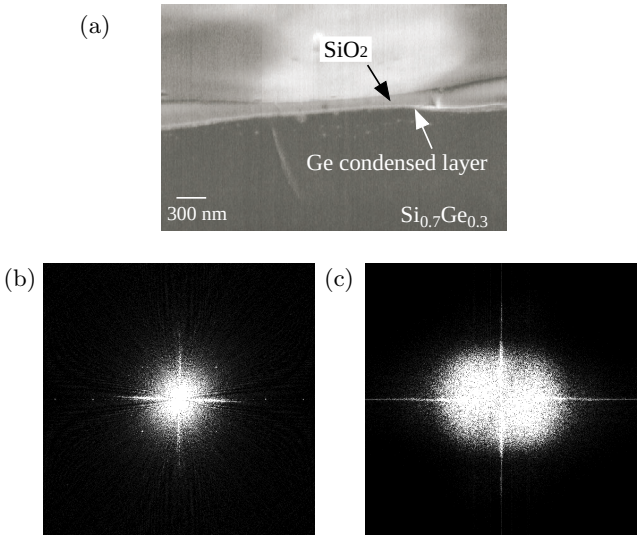

Fig. 3: (a) Cross-section of the strained-Si/SiGe oxidized at 850°C for 5 hours in wet-O_2. Fourier transformed patterns taken from strained-Si wafer. (b) before (c) after oxidation.

Acknowledgements

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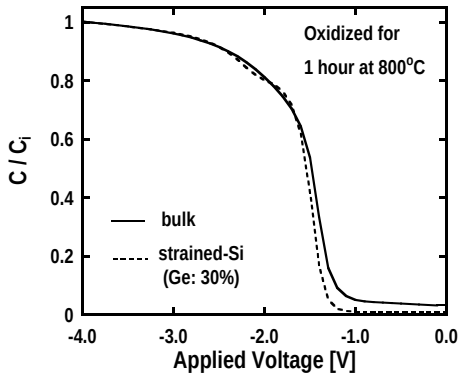

Fig. 4: High frequency C-V characteristics of strained-Si (dashed line) and bulk-Si (solid line) MOS capacitor.

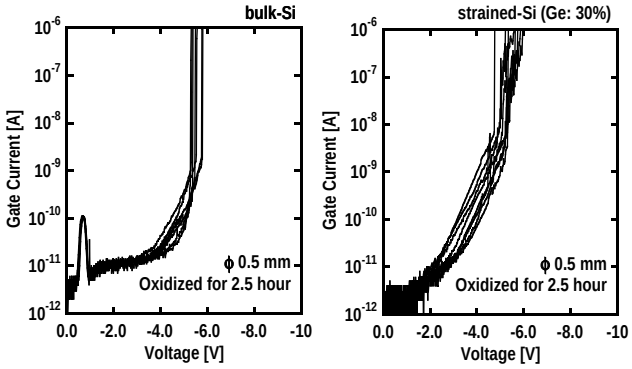

Fig. 5: I-V characteristics of thermally grown oxide films on (a) bulk-Si and (b) strained-Si.

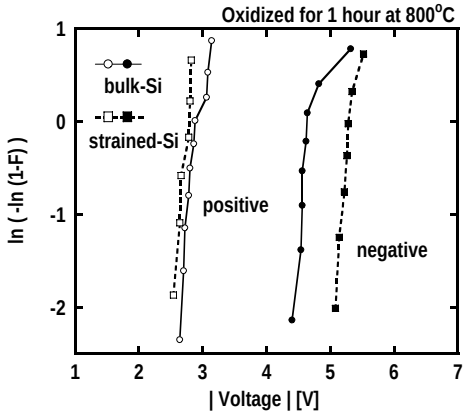

Fig. 6: Weibull plots of breakdown voltage taken from bulk-Si and strained-Si samples oxidized for 1 hour at 800°C.