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GaAs-MISFETs with nm-Thin Gate Insulating Films Formed by Oxi-Nitridation Process

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1. Introduction

A metal/insulator/semiconductor (MIS) gate is essentially better than a Schottky gate in scalability, high temperature and single power source operation, availability of an enhancement mode device, etc. However, due to difficulty of obtaining a MIS gate compound semiconductor FET of good performance, the MIS gate technique is still under resarch situation. In-situ process in a high vacuum or liquid phase is the main process which is investigated by many researchers. This paper describes excellent performance GaAs MISFETs which were fabricated by a combination of ex-situ oxidation by UV & ozone and nitrogen plasma processes (oxi-nitridation).

2. Oxi-Nitridated GaAs Layers

The oxidated GaAs layer is composed of Ga-oxide which contains plenty of As-oxide. The nitrogen plasma process drives out As from, and incorporates N into, the layer and changes its main composition into Ga-oxi-nitride.

Figure 1 shows a cross-sectional TEM image of an IS junction which was formed on a (100) GaAs surface by 8hrs nitrogen plasma treatment after 8hrs UV & ozone oxidation [1]. A very flat interface with very little crystallographic disorder is observed. Photoluminescence intensity of the oxidated GaAs surfaces increases by the subsequent nitridation [1]. MIS diode characteristics of thus formed IS interface suggested existense of very little interface charges [2].

3. Fabrication Process

GaAs-MISFET with oxi-nitridated gate insulating layer was fabricated using n/S.I. GaAs wafers. The epitaxial layer has a donor density of $3.0\times10^{17}\mathrm{cm}^{-3}$ and a thickness of 0.4μm. Figure 2 shows the structure of the GaAs-MISFET. Native oxide layer on the surface of the substrate was removed by buffered hydrofluoric acid etching and the epitaxial layer was thinned to 0.3μm by an etchant ($H_3PO_4:H_2O:H_2O_2=4:90:1$) in order to reduce the mesa-step-height. The source and drain electrodes ware formed by evaporating AuGe/Ni and sintered at 360 $^\circ$C for 1 min. The mesa etching and the recess etching were carried out by using the same etchant. The channel thickness of the recessed portion is 0.18μm. In forming the insulating layer, the recessed surface was oxidized first for 4 hrs, and then nitridated (RF power 50W, N_2 flow rate 10sccm). Thickness of thus formed inslating layer is about 8nm. Al was evaporated as the gate electrodes finally.

4. Electric Performance

Figure 3 shows drain current I_D versus drain voltage V_D, at gate bias V_G from -2V to 3V in 0.5V step, of 1 μm gate length GaAs-MISFETs with oxide (a) or oxi-nitridated insulating layer (b), respectively. In Figure 3(a), pinch-off is not good, hysteresis was obseved similar to the MOSFET we reported in 2001 [3]. While in Figure 3(b), pich-off is improved and higher transconductance is obtained. Hysteresis is completely removed by the 2hrs nitridation.

Figure 4 shows gate diode characteristics of the MISFETs with such oxi-nitridated insulating layer . The leakage current in the reverse bias region is decreased depending on the nitridation times. The nitridation suppressed the leakage current up to 3 orders of magnitude compared to the simple oxide gate.

Gate voltage dependence of transconductance of the MISFETs with different nitridation time, at drain voltage V_D of 5V are shown in Figure 5. The MOSFET sample with no nitridation has a maximum transconductance of 60 mS/mm. The 2hrs nitridation MISFET sample has that of 110 mS/mm. Maxmum transconductance $g_{m,Max}$ versus gate length L_G is shown in Figure 6. The dependence of $g_{m,Max}$ on L_G becomes clear by the 2hrs nitridation.

5. Conclusions

We demonstrated GaAs-MISFET with oxi-nitridated gate insulating layer. It indicated higher leakage current suppressing performance than the oxide gate device. The GaAs-MISFET shows good pinch-off and higher transconductance with no dip at flatband voltage.

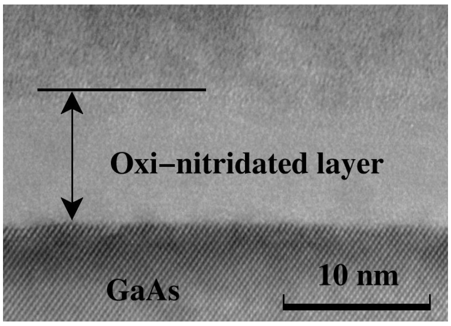


Fig. 1 Cross-sectional TEM image of the oxi-nitridated GaAs layer formed by 8hrs nitridation after 8hrs oxidation

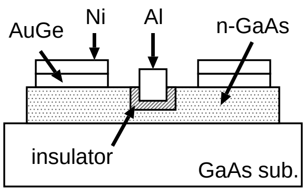
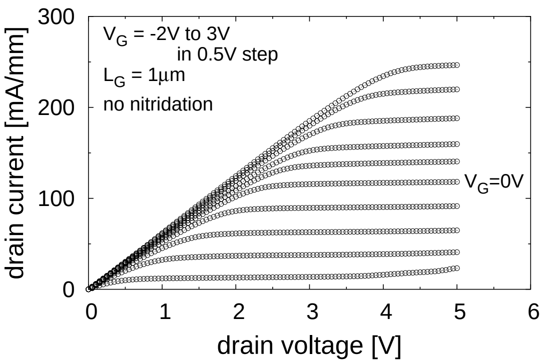
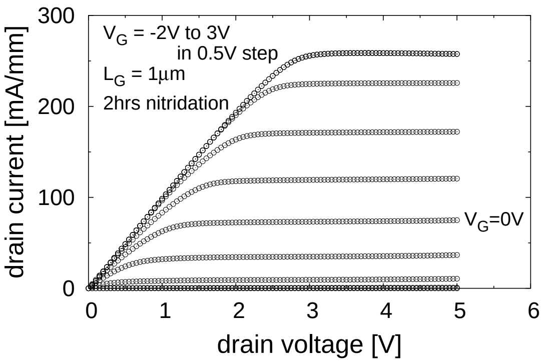


Fig. 2 Structure of GaAs-MISFET, $N_D = 3.0 \times 10^{17} cm^{-3}$, thickness of channel is 0.18μm.



(a)



(b)

Fig. 3 Normarized DC characteristics of 1 μm GaAs-MISFET with 4hrs oxidation (a), 2hrs nitridation after 4hrs oxidation (b).

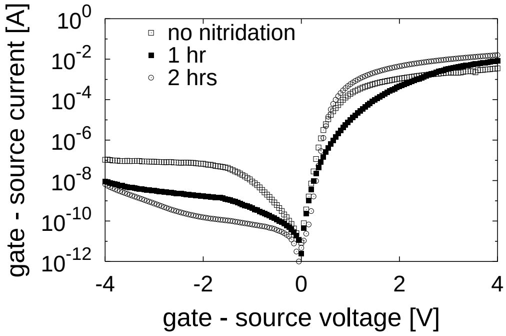


Fig. 4 MIS diode characteristics

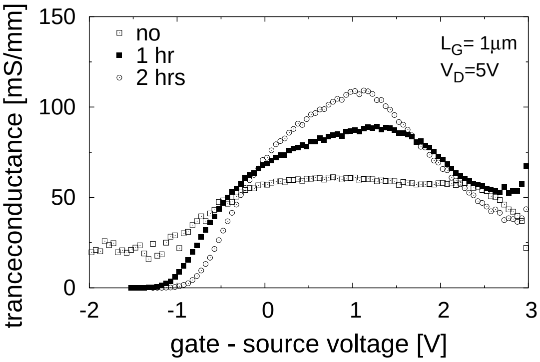


Fig. 5 Transconductans with different nitridation time at drain voltage of 5V

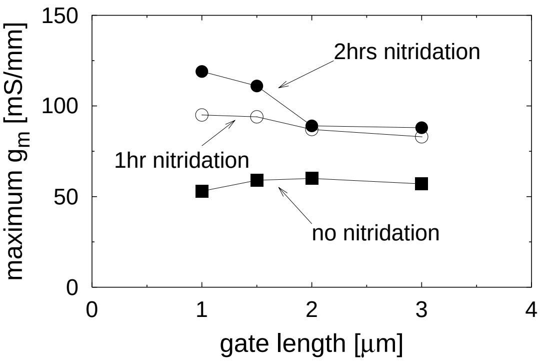


Fig. 6 Gate length dependence of maximum transconductans with different nitridation time

References

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[3] M.Nasuno, et al. *TECNICALREPORT OF IEICE*, ED2002-188, pp.17-22, Aug,2002.

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