

Side Gating Phenomenon in GaAs Quantum Wire Transistors

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1. Introduction

It is generally believed that a new nanoelectronics will emerge in near future with unprecedented integration densities and speed-power performances beyond the scaling limit of Si CMOS LSIs. Ultrahigh density and ultra low power III-V quantum (Q-)LSIs is one candidate for such. As a realistic approach for high density integration of III-V quantum devices such as quantum wire transistors (QWRTrs) and single electron transistors (SETs), our group has recently proposed a hexagonal binary decision diagram (BDD) quantum circuit approach [1,2] where quantum transport within a hexagonal nano-wire network is controlled by nm-scale Schottky gate.

For high density integration of III-V gated quantum devices, one critical issue that has not been addressed so far is the side gating related to device isolation. It is well known that side gating limits the achievable integration density in III-V LSIs based on MESFETs and HEMTs[3].

The purpose of the present paper is to investigate experimentally the side gating behavior of GaAs QWRTrs controlled by wrap gates (WPGs)[1,2].

2. Experimental

The structure of a QWRTr device with a WPG used in the experiment is schematically shown in **Fig. 1 (a)** together with arrangement and structure of the test Schottky side gate. The cross-sectional structure of the wafer used to fabricate devices is shown in **Fig. 1 (b)**. The wafer was grown by MBE, and the device was fabricated using electron beam lithography and wet chemical etching. Typically, the nanowire width was 500 nm at the mesa top.

Important parameters for the side gating study were the etched thickness for device isolation, t_e , and the distance between side gate edge and the nanowire edge, d_{sg} . For high density integration, smaller values of t_e and d_{sg} are desirable, since a smaller value of t_e gives a quasi-planar structure preferable for wiring. In this study, two cases of $t_e = 95$ nm (AlGaAs surface) and $t_e = 210$ nm (GaAs buffer surface) were compared. The value of d_{sg} was changed between 400 nm and 1,000 nm, since it was rather difficult to realize smaller values of d_{sg} reproducibly on the non-planar structure. In order to avoid statistical variations of parameters other than d_{sg} , devices having different values of d_{sg} were produced on the same chip, undergoing the same processing steps. A plan-view SEM image of a completed device is shown in **Fig. 1 (c)**. Devices showed clear conductance quantization at low temperatures.

However, side gating was investigated in this study at room temperature, since our goal is to realize quantum effects at room temperature. So far, a similar device has shown quantization up to 100K[4]. Additionally, a key feature of our BDD quantum circuit is that it works correctly even at room temperature at a sacrifice of the power delay product [1,2]. Side gating characteristics were also measured in large amplitude FET modes to clearly see potential problems, although QWRTrs are usually operated at small voltages in the linear region.

3. Results and discussion

Observed side gating behavior

The fabricated devices showed different side gating behavior, depending on the values of t_e and d_{sg} . An example showing a strong side gating is shown in **Fig. 2 (a)** and **(b)**. When a negative voltage was applied to the side gate, the channel current was very much reduced even for relatively small voltage values. This means the neighboring GaAs devices on one chip interact greatly when the device separation is small. As shown in **Fig. 3 (a)**, side gating effect became much smaller for large distance, d_{sg} . The observed behavior is summarized in **Fig. 3 (b)** in terms of the side gate transconductance, g_{msg} , which is defined as $g_{msg} = dI_{ds}/dV_{sg}$ ($V_g, V_{ds} = \text{const}$). Here I_{ds} , V_{ds} , V_g and V_{gs} are the drain current, drain voltage, gate voltage and side gate voltage, respectively. There exist three Regions A, B and C of side gating characteristics. A is

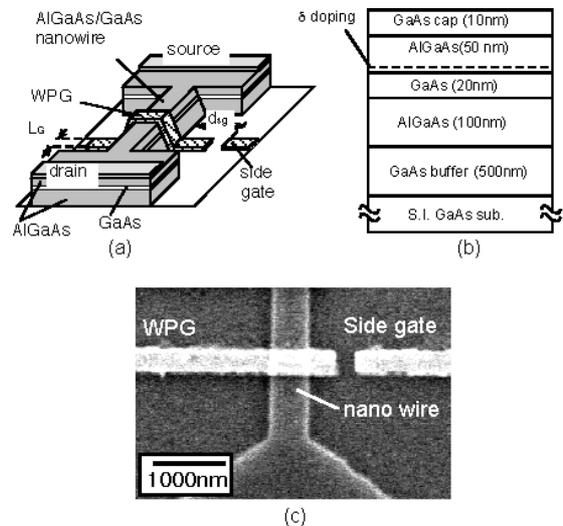


Fig.1 (a) Structure, (b) wafer cross-section and (c) SEM image of a WPG QWRTr with a side gate.

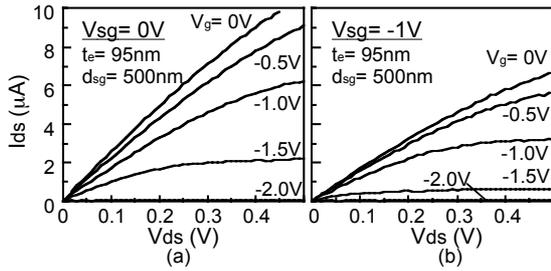


Fig. 2 I_{ds} - V_{ds} curves showing strong side gating. (a) $V_{gs} = 0V$ and (b) $V_{gs} = -1V$.

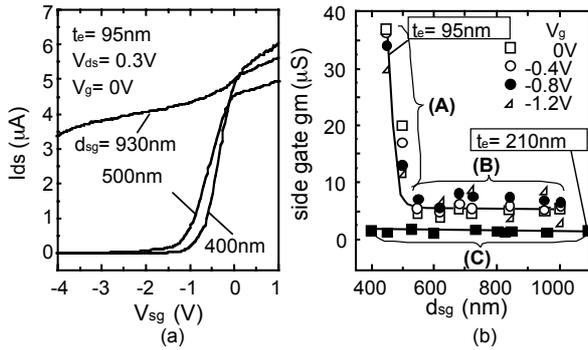


Fig. 3 (a) d_{sg} dependence of I_{ds} - V_{sg} curves and (b) a summary of side gating behavior showing three Regions A, B and C.

the region with strong side gating with a strong d_{sg} -dependence whereas B and C are the regions of weak and d_{sg} -independent side gating. It is seen that Region C with $t_e = 210$ nm gives only very small side gating for a wide range of d_{sg} and seems satisfactory for integration.

Mechanism of side gating

In order to clarify the side gating mechanism, V_{sg} dependence of I_{ds} - V_g characteristics are summarized in **Fig. 4 (a)**, **(b)** and **(c)** for the devices in the Regions A, B and C, respectively. As seen in **Fig. 4**, the side gate acts almost like the main gate in the device in Region A, whereas side gating behavior of devices in Regions B and C is weak and similar, roughly causing parallel shifts of curves. Previously, side gating in MESFETs were correlated with the side gate leakage current, and one of the present authors [3] explained this in terms of avalanche break-down due to surface state filling. To explore such a possibility, the measured leakage currents between the main gate and the side gate are shown in **Fig. 4 (d)**. There is no indication of impact ionization here. In fact, leakage current is the largest in the device in Region C.

Our proposal for the side-gating mechanism is shown in **Fig. 5**. When both of t_e and d_{sg} are small, sideway depletion can proceed into the lower barrier region of the device and deplete the channel. When either or both of t_e and d_{sg} are large, then sideway depletion cannot directly deplete the channel, and weakly modulate the potential of

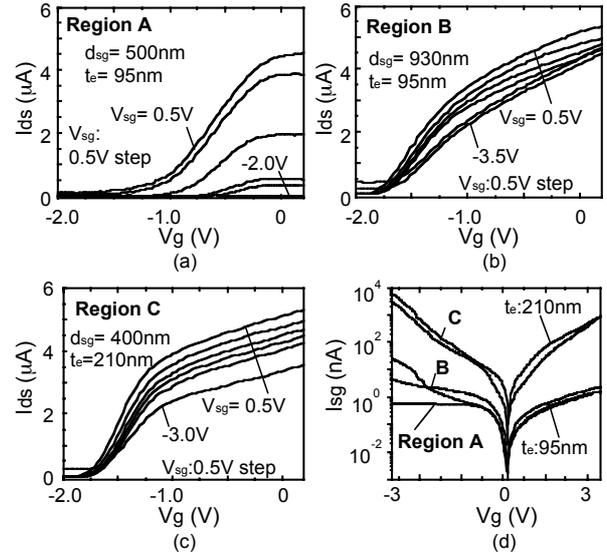


Fig.4 V_{sg} dependences of I_{ds} - V_g curves for the devices in (a) Region A, (b) Regions B and C. (d) Measured leakage currents for these devices.

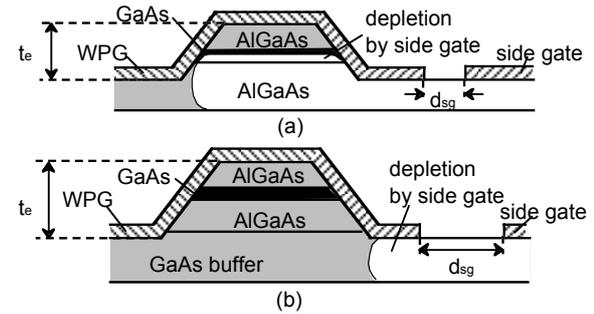


Fig.5 Proposed model for side gating (a) for devices in Region A and B, and (b) for devices in Region C.

the neutral region of the lower barrier, causing a change in the threshold voltage. The latter is similar to the substrate bias effect which is weakly dependent on the distance.

4. Conclusions

Side-gating behavior of GaAs quantum wire transistors was investigated for the first time, and its mechanism was explained. Etching depth for device isolation was found to be a key parameter for successful device isolation.

Acknowledgement

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