Formation of Ge Quantum dots by Selective Oxidation of SiGe alloys for Single-Electron Devices

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1. Introduction

As further development of the well established CMOS technology starts to reach it limits, more and more new technologies are being suggested which promise to continue the trend to smaller, faster, low-power, and cheaper. Among these new technologies, single-electronics is particularly interesting. The advent of advanced nanometer technology has paved the way for single electron (SE) devices into low power and fast integrated circuits. Crucial for an industrial success of single-electron devices is operation at room temperature, manufacturability with established, economical, and reproducible methods, and immunity to random background charges. All devices so far reported violate one or more of the above stated requirements. Based on the results of current research, it can be known that the development is still at a stage in which electron beam (E-beam) lithography and reactive ion etching are being used to form quantum dots [1]-[3].

In this work, we explored a novel method that is compatible to the prevailing CMOS technology for forming germanim quantum dots using selective oxidation of Si_{1-x}Ge_x alloys. It is known that Si will be preferentially oxidized during high-temperature oxidation of Si_{1-x}Ge_x alloy; and Ge atoms will segregate out and pile up along the SiGe/SiO₂ interface [4],[5]. Therefore, it can be expected that the atomic-scale Ge quantum dots would be formed by the Ge atom segregation and agglomeration, instead of by the resolution of advanced E-beam lithography and etching technology.

2. Sample Fabrication

The fabrication of germanium quantum dots started from a silicon-on-insulator (SOI) wafer prepared by separation by implanted oxygen (SIMOX) technology. The thickness of the surface Si layer and the buried oxide layer are 208 and 375 nm, respectively. The top silicon layer was thinned to 22 nm by repeated thermal oxidation and subsequent wet etching processes. Then a tri-layer (a 10 nm Si buffer layer/ a 8 nm strained Si_{0.95}Ge_{0.05}/ a top-most 2 nm Si cap layer) was grown by ultra-high vacuum chemical vapor deposition (UHVCVD) at 550 °C. The top Si/Si_{0.95}Ge_{0.05}/Si multilayer was patterned using electron-beam (EB) lithography and sequential dry etching to form narrow wire structures as shown in Fig.1. The width of the wires was 20~50 nm while the length varied in the range of 50-120 nm (Fig. 1(b)). Next, the buried oxide is etched beneath the wires transforming them into free-standing bridges. Subsequently, thermal oxidation was performed to completely oxidize the narrow Si/Si_{0.95}Ge_{0.05}/Si wires and hence, Ge dots were expected to be wrapped in the top and the buried oxides by Ge segregation during oxidation process (Fig. 1(c)).

3. Experimental Results and Discussion

It is reasonable to expect that the size and distribution of the Ge dots formed by selective oxidation of Si1-xGex are determined by the Ge atoms' segregation and agglomeration, which may differ according to the germanium content in Si_xGe_{1-x} layer and conditions of thermal oxidation process (temperature and time). Fig. 2(a) shows the plane-view and cross-sectional transmission electron microscopy (TEM) of the Si_{0.95}Ge_{0.05}/Si layer after 900 °C thermal oxidation for 10 minutes, where Si_{0.95}Ge_{0.05} was just being oxidized while the underlayer Si is unconsumed. It is clear to see that there is Ge pileup along the SiO₂/Si interface and the Ge agglomeration is in the initial stage with an average dot diameter of 9.2 \pm 6.8 nm and density of 150 /0.1 μ m². It can be expected that additional thermal oxidation or annealing would provide energy required for Ge atom agglomeration and movement. A smaller Ge dot size (6.5±3.4 nm) is obtained for Si_{0.95}Ge_{0.05}/Si layer after 20 minute oxidation at 900 °C with the average density of ~600/0.1 μ m² as shown in Fig. 2(b). The dot size and uniformity of the Ge dot is much improved by the additional thermal process as summarized in Fig. 3. The fabrication of Ge single-electron transistors with Ge dots formed by selective oxidation of $Si_{1-x}Ge_x$ is undergoing and the electrical properties will be characterized.

4. Conclusions

A simple and novel method for forming germanium quantum dots is proposed for application in single electron transistors or optical devices. The formation of atomic-scale germanium dots is realized by selective oxidation of SiGe layer while the size and distribution of the germanium dots are determined by conditions of thermal oxidation process.

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Fig. 1 (a) Schematic of the narrow wire structure, (b) SEM micrograph of a narrow wire, (c) Ge dots formation by selective oxidation of $Si_{1-x}Ge_x$ and Ge segregation.





Fig. 2 TEM pictures of $Si_{0.95}Ge_{0.05}$ (source/drain region) after (a) 11 min. and (b) 20 min. oxidation at 900 $^{\circ}C.$

2(b)



Fig. 3 Ge dot size and variation change with oxidation time.