SOI SRAM / DRAM Cells for 0.5 Volt Operation
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Abstract
A 4T SRAM cell utilizing the ‘Self-Body-Biased’ (‘SBB’) SOI MOSFET structure and an SOI DRAM gain cell, both operating at low supply voltage, are described. Both cells actively exploit the SOI body region as one of the cell components. Mixed-mode simulation reveals that both memory cells properly operate under a supply voltage of as low as 0.5 V.

Introduction
The ‘SBB’ SOI MOSFET [1] utilizes the expansion of the gate depletion layer beneath the auxiliary T-shaped gate electrode in order to modulate the body potential of the SOI MOSFET. This scheme is realized because there exists a potential barrier between the body region of the ‘SBB’ SOI MOSFET and the body diffusion terminal (‘depletion isolation effect’ [2]).

In this report the author describes the operation of a novel 4T SRAM cell using the ‘SBB’ SOI MOSFET structure [3]. The body region of the ‘SBB’ SOI MOSFET with an ‘H-shaped’ gate electrode is used as a load resistor in the inverter pair of the SRAM cell. A novel SOI DRAM gain cell [4] is also described. Both memory cells can be fabricated using conventional 1poly logic processes and can properly operate under a supply voltage of as low as 0.5 V. Therefore these memory cells are absolutely suitable for embedded memories intended for portable, battery-driven applications.

4T SRAM cell with ‘H-gate’ ‘SBB’ SOI MOSFETs
Figure 1 illustrates (a) the plan view and (b) the equivalent circuit of the proposed ‘SBB’ SOI MOSFET with an ‘H-shaped’ gate electrode. Body diffusion at the MOSFET side (BODY2) is the same as the body diffusion of the conventional body-tied SOI MOSFETs. As in the case of ‘T-gate’ ‘SBB’ SOI devices [1], the gate depletion layer extending in the ‘low Na’ region plays an important role in modulating the conductivity between BODY1 and BODY2. Thus by changing the impurity concentration in the ‘low Na’ region and the auxiliary gate geometry (i.e., Lb and Wb), the desired resistance should be realized.

In order to obtain the characteristics of the proposed ‘H-gate’ ‘SBB’ SOI MOSFET the author has utilized the modified double gate structure shown in the inlet of Fig.2. It has shallow drain diffusion as well as shallow source diffusion, enabling the body potential to be controlled through the remaining body region via BODY1 and BODY2 terminal depending on gate voltages (Vg).

Figure 2 shows the Vg dependence of IBODY1-BODY2 of the proposed device with various ‘low Na’ concentration. This relationship indicates that the conductivity between BODY1 and BODY2 is determined primarily by the impurity concentration in the ‘low Na’ region over the gate voltage ranging from 0 to 1.5 V.

Figure 3 (a) shows the circuit diagram of the proposed 4T SRAM cell, and Fig.3 (b) is its calculated transfer curve. This transfer curve clearly indicates the existence of the two stable cross-point around VSN1=0 V and 0.5 V under operating voltage of 0.5 V. Data shown in Fig.4 indicate that threshold voltage setting (i.e., ‘high Na’ impurity concentration) is a key parameter for its stable operation at a low supply voltage whereas there is only weak dependence of the ‘low Na’ value. Fig.5 (b) clearly shows the cooperative nature of the BODY1-BODY2 conductance of the ‘H-gate’ ‘SBB’ SOI MOSFET to its inverter operation as compared with a fixed external load resistor.

SOI DRAM gain cell
Figure 6 illustrates (a) the cross sectional view, (b) the equivalent circuit, and (c) bias conditions of the proposed SOI DRAM gain cell. It is basically a partially depleted SOI MOSFET with two body terminals (RLW and RBL), whose source / drain diffusions do not extend to the SOI-BOX interface. The conductance between RLW and RBL is dependent on SN potential through the extension of depletion layer formed at the SN pn junction. SN potential is modulated by WBL voltage through the MOSFET switch activated by WWL voltage. Note that bipolar data line (bit line) voltage is not required in the operation of the proposed SOI DRAM gain cell whereas it is inevitable in other SOI gain cells [5,6].

The waveforms shown in Fig.7 illustrate the SOI DRAM gain cell operation. Simulation clearly indicates that ISBL in the case of “0” read is almost five times as large as ISBL in the case of “1” read, and substantially large ISBL (of order of μA/μm) can be obtained in the read operation of the proposed gain cell. Note that overlap capacitance between SN diffusion and WWL (=WWL for another cells) affects its retention characteristics.

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References
Fig. 1 (a) Plain view and (b) equivalent circuit of the proposed ‘H-gate’ ‘SBB’ MOSFET structure.

Fig. 2 $V_g$ dependence of $I_{BODY1-BODY2}$ of the proposed device with various ‘low Na’ concentration.

Fig. 3 (a) Circuit representation of the proposed 4T SRAM cell and (b) its calculated transfer characteristics obtained by mixed-mode simulation.

Fig. 4 (a) ‘High Na’ and (b) ‘low Na’ dependence of the ‘H-gate’ ‘SBB’ inverter.

Fig. 5 $V_{BODY2}$ voltage dependence of the transfer characteristics of the ‘H-gate’ ‘SBB’ inverter.

Fig. 6 (a) Cross-sectional view, (b) equivalent circuit, and (c) bias conditions for the proposed SOI DRAM gain cell.

Fig. 7 Simulated readout waveforms of the proposed SOI DRAM gain cell. Inlet is a time evolution of $V_{SN}$ during write operation.