# A Complete Surface-Potential-Based SOI-MOSFET Model for Circuit Simulation

D. Kitamaru, Y. Uetsuji, and M. Miura-Mattausch

Graduate School of Advanced Sciences of Matter, Hiroshima University

1–3–1, Kagamiyama, Higashi-Hiroshima, 739–8530, Japan

 $Phone: \ +81-824-24-7637 \ \ Fax: \ +81-824-22-7195 \ \ E-mail: \ mmm@hiroshima-u.ac.jp$ 

## 1. Introduction

SOI-MOSFET is a candidate for next generation integrated circuit technology due to its reduced junction capacitances and improved subthreshold swing [1]. However, a robust circuit simulation model is still missing, and a bulk-MOSFET model, sacrifying specific features of the SOI-MOSFET, is mostly applied. Problem of existing SOI-MOSFET models is their difficulty to get convergence. The main reason for the unstability in circuit simulation may be attributed to disturbance of the charge conservation [2]. Thus our aim here is to develop a model for fully-depleted SOI-MOSFET, which considers device features explicitly as well as preserves the charge conservation. For this purpose the model is developed based on the surface-potential description, and is named HiSIM-SOI.

## 2. Theoretical Investigation

Figs. 1a and 1b show a schematic of the SOI-MOSFET and its energy-band diagram along the vertical direction of the channel. The drain current flows in the inversion layer of  $\phi_{s,SOI}$  at the surface-SOI. A basic equation of the SOI-MOSFET for the applied gate voltage  $(V_{\rm gs})$  is

$$V_{\rm gs} - V_{\rm fb} - \Delta V_{\rm th} = \phi_{\rm s, BULK} - \frac{Q_{\rm BULK}}{C_{\rm BOX}} - \phi_{\rm SOI} - \frac{Q_{\rm BULK} + Q_{\rm SO}}{C_{\rm FOX}}$$
(1)

where  $V_{\rm fb}$  and  $\Delta V_{\rm th}$  are the flat-band voltage and the threshold voltage ( $V_{\rm th}$ ) shift from a long-channel transistor, respectively [3].  $C_{\rm BOX}$ ,  $C_{\rm FOX}$ , and  $\phi_{\rm SOI}$  are the BOX capacitance, the gate-oxide capacitance, and  $\phi_{\rm s,SOI}$ - $\phi_{\rm b,SOI}$ .  $Q_{\rm BULK}$  and  $Q_{\rm SOI}$  are charges in the bulk and in the SOI layer. Here two important tasks to be considered in developing an analytical SOI-MOSFET model arises. : (1)Three different surface potential values ( $\phi_{\rm s,SOI}$ ,  $\phi_{\rm b,SOI}$ ,  $\phi_{\rm s,BULK}$ ); (2)Two additional device parameters (thickness of BOX, and impurity concentration of BULK) (i) For the task (1):

Fig. 2 shows simulated electron concentrations in the channel with the 2D-device simulator MEDICI [4] as a function of  $V_{\rm gs}$ . The values both at the source side and the drain side are shown. If the electron concentration exceeds the impurity concentration  $N_{\rm sub}$ , it gives the inversion condition. It can be seen that both depletion and inversion conditions occur at both SOI and bulk surfaces.

Whereas the inversion condition never occurs at the back side of SOI under normal operation conditions. Combinations of all these conditions have to be considered in describing the charges appear in Eq. (1). All charges are functions of the three surface potentials. They are obtained by solving the Poisson equation in 1D to the vertical direction together with Eq. (1), iteratively. This is a key to preserve the charge conservation. Till now the iteration requires about twice as much calculation time as bulk HiSIM [5]. However, it can be reduced by restricting conditions considered. For example disregarding the inversion condition at the bulk-surface simplifies the description, of which the contribution is small. (ii) For the task (2):

(ii) For the task (2):

Different from the bulk-MOSFET, the SOI-MOSFET includes two additional device parameters, which are also very sensitive for determining device characteristics. All these values have to be extracted independently from very beginning of parameter extraction. This can be done with  $V_{\rm th}$  as the bulk-MOSFET case [3]. However, the  $V_{\rm th}$ description is not single but differs for different conditions considered in (i). Fig. 3 demonstrates that 4 independent regions are distinguished in the  $V_{\rm th}$  characteristics as a function of the bulk voltage ( $V_{\rm bs}$ ) [6]. Each region is mainly determined by a specific device parameter. We very exploit the characteristics of the SOI-MOSFET for the parameter extraction.

#### 3. Calculation Results

The surface potential values calculated by HiSIM-SOI are verified with MEDICI results. Calculated current-voltage characteristics are compared in Fig. 4 with measurements for the gate length  $L_{gate}$  of  $10\mu$ m. For the calculation, parameter values relating to the mobility are extracted with measured current-voltage characteristics. The conventional universal mobility description for the bulk-MOSFET [5] was applicable without any modification. Calculated ring oscillator characteristics is demonstrated in Fig. 5 for  $L_{gate}$  of  $2\mu$ m.

## 4. Conclusion

Circuit simulation model for fully depleted SOI-MOSFET has been developed based on the complete surface-potential description for the first time. The model is implemented into the circuit simulator SPICE and stable circuit simulation has been proven.

### Acknowledgement

Authors would like to express their thanks to L. Weiss and U. Feldmann (Infineon Technologies), and S. Baba (Oki Electric Industry) for their support in accomplishing this work. A part of this work was supported by the New Energy and Industrial Technology Department Organization, Japan.

## References

- Ran-Hong Yang, Abbas Ourmazd, and K. F. Lee, IEEE Trans. Elec. Dev., 39, 1704, 1992.
- [2] D. Suh and J. G. Fossum, IEEE Trans. Elec. Dev., 42, 728, 1995.
- [3] M. Miura-Mattausch, U. Feldmann, A. Rahm, M. Bolu, and D. Savignac, IEEE Trans. CAD/ICAS, 15, 1, 1996.
- [4] MEDICI User's Manual
- [5] HiSIM User's Manual, http://www/starc.or.jp.
- [6] D. Kitamaru, Master's degree dissertation, Hiroshima University, March 2003.



Figure 1: (a) Schematic of the SOI-MOSFET cross-section, and (b) Band diagram along the vertical direction to the channel.



Figure 2: Simulated electron concentrations in the channel with the 2D-device simulator MEDICI as a function of the gate voltage  $V_{\rm gs}$  at three different surfaces shown in Fig. 1b. Values both at the source edge and the drain edge are depicted. The horizontal dashed lines show the impurity concentration in the SOI layer,  $N_{\rm sub,SOI}$ , and that in the bulk,  $N_{\rm sub,BULK}$ .



Figure 3: Threshold voltage  $(V_{\rm th})$  as a function of the bulk voltage  $(V_{\rm bs})$ . Different numbers give different combinations of three different surface conditions mentioned (i). Each combination gives different  $V_{\rm th}$  description [6].



Figure 4: Comparison of calculated result with measured (a) drain current  $(I_{\rm ds})$  as a function of the gate voltage  $(V_{\rm gs})$  and (b)  $I_{\rm ds}$  as a function of the drain voltage  $(V_{\rm ds})$ .



Figure 5: Simulated ring ocillator period for  $L_{\text{gate}}=2\mu$ m as a function of time with HiSIM-SOI. For the simulation extrinsic capacitances are ignored to test convergence.