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High Performance Buried Gate Surrounding Gate Transistor (BG-SGT) for Future Three-Dimensional Devices

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1. Introduction

Surrounding Gate Transistor (SGT) have received much attention as future devices for DRAM, Flash EEPROM and conventional CMOS applications [1-3]. The SGT arranges source, gate and drain vertically. Therefore, the occupied area of SGT can be smaller than that of planar MOSFET. Since gate electrode surrounds the silicon region, the occupied area of SGT depends on minimum feature size F and thickness of gate. On the other hand, that of planar MOSFET depends on only minimum feature size F. The ratio of gate electrode to occupied area becomes larger with scaling down about minimum feature size F. The high packing ability of SGT can not take advantage by increase of the ratio of gate electrode to occupied area. Furthermore, decreasing pillar size of SGT is necessary to achieve ideal subthreshold slope with fully depleted condition. However, decreasing pillar size of conventional SGT lead to decrease of drive current with increase of source and drain (S/D) resistance.

In this paper, we propose Buried Gate SGT (BG-SGT) to overcome both the problems mentioned above. BG-SGT is able to shrink the ratio of gate electrode to occupied area with buried gate structure. Moreover, as decreasing body pillar size, BG-SGT can realize ideal subthreshold slope and suppression of increase of S/D resistance with vertical spread S/D structure.

2. BG-SGT Structure

Fig.1 shows the schematic view of a BG-SGT. The BG-SGT, as well as the conventional SGT, arranges source, gate, and drain vertically. In the BG-SGT, the gate oxide and the gate electrode are buried inside silicon pillar. In comparison with the conventional SGT, as the gate electrode thickness outside silicon pillar decreases, the BG-SGT can realize the decrease of the occupied area. Moreover, the top pillar size is bigger than the body pillar size. This structure is the vertical spread S/D structure, as well as raised S/D structure for the planar transistor. Fig.2 shows the fabrication steps of the BG-SGT. In the fabrication steps, the buried gate region is formed following possible process: The pillar silicon island is formed by conventional silicon trench etching technology. The silicon nitride and polysilicon are deposited between the bottom of pillars. The silicon nitride spacers are formed at the sidewalls of the top of pillars. The top and bottom of pillars were covered with silicon nitride (Fig.3(a)). After the removal of polysilicon, buried gate region is formed by isotropically etching (Fig.3(b)). Thus, the buried gate region is carried out.

3. Results and Discussion

A. High packing Ability

Fig.4 shows a comparison between the occupied areas by planar transistor, conventional SGT and BG-SGT. The feature size is 100nm. Each gate oxide thickness and gate electrode thickness are equal to 1.1nm and 45nm, respectively [4]. In this case, the body pillar size of BG-SGT is 20nm. By using this BG-SGT, the occupied area can be shrunk to 52.7 % of that of the conventional SGT and to 37.5 % of that of planer transistor.

Fig.5 shows dependence of occupied area on body pillar size of BG-SGT. The occupied area of BG-SGT decrease with further decrease in body pillar size. As the body pillar size decreases to less than 20nm, the occupied area of BG-SGT can be shrunk to less than 52.7 % of that of the conventional SGT. Therefore, the BG-SGT can realize the high-shrinkage feature.

B. Subthreshold Characteristics

Fig.6 shows the dependence of subthreshold swing S on body pillar size for conventional SGT and BG-SGT. The channel length is 200nm and drain voltage is 0.05V. It is found that the subthreshold swing S for BG-SGT with the body pillar size of 50 nm is 60 mV/dec and smaller than that for conventional SGT, i.e., 68 mV/dec. By decreasing the body pillar size, the subthreshold swing S becomes smaller and body becomes fully depleted condition. Therefore the BG-SGT with the body pillar size of 50 nm reaches the ideal value.

C. Suppression of Increase of S/D Resistance

Fig.7 shows dependence of drive current on body pillar size for BG-SGT and conventional SGT. The drive current of BG-SGT increases with body pillar size scaling down, while that of conventional SGT decreases. It is explained by Miyano et al [5] that current drivability of SGT will increase as the body pillar size decreases. BG-SGT suppresses the increase of S/D resistance with body pillar size scaling down by vertical spread S/D structure. Therefore, BG-SGT can enhance drive current.

Fig.8 shows comparison of I_D-V_D characteristics between BG-SGT and conventional SGT at body pillar size of 10nm. For $V_G=V_{th}+1.0$, drive current of BG-SGT is 15% larger than that of conventional SGT. For conventional SGT, decreasing body pillar size lead to decrease of drive current with increase of S/D resistance. Thus, it is very important to use vertical spread S/D structure of BG-SGT with body pillar size scaling down.

4. Conclusions

We have demonstrated BG-SGT for high performance transistors. BG-SGT is able to shrink the ratio of gate electrode to occupied area with buried gate structure. Therefore, BG-SGT can realize the high-shrinkage feature. Moreover, BG-SGT can realize suppression of increase of S/D resistance with vertical spread S/D structure even if body pillar size decreases. And decreasing body pillar size leads to steep subthreshold slope. Owing to these features, BG-SGT is extremely attractive for future three-dimensional devices.

References

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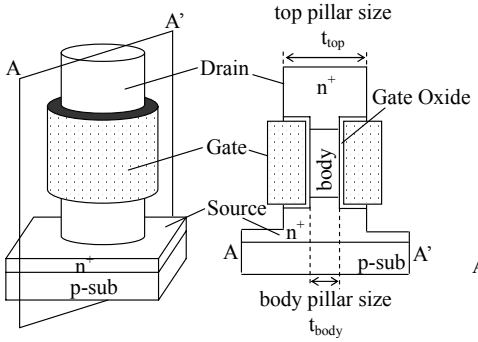

Fig.1 Buried Gate SGT (BG-SGT) schematic view

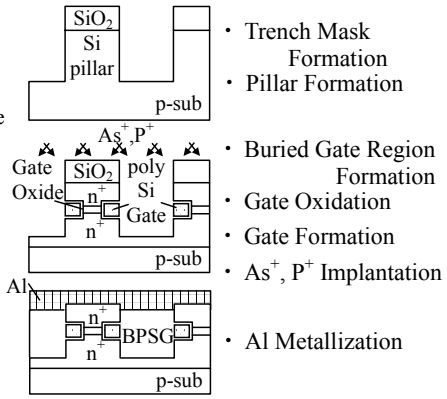

Fig.2 Fabrication steps of the BG-SGT

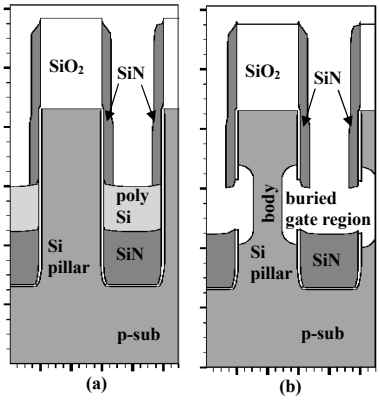

Fig.3 Results of process simulation of buried gate region formation

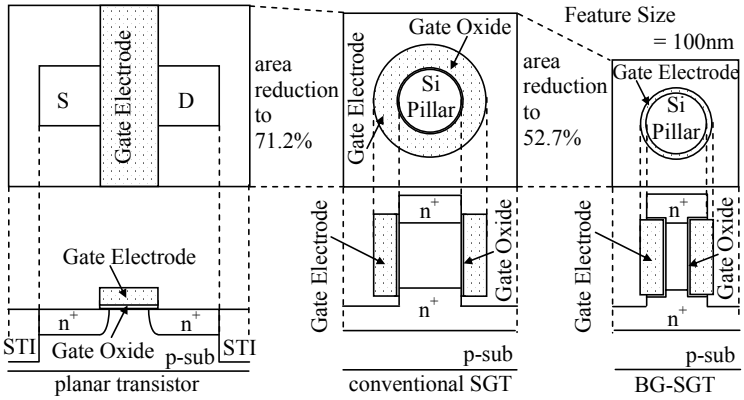

Fig.4 Comparison between the areas occupied by planar transistor, a conventional SGT and BG-SGT.

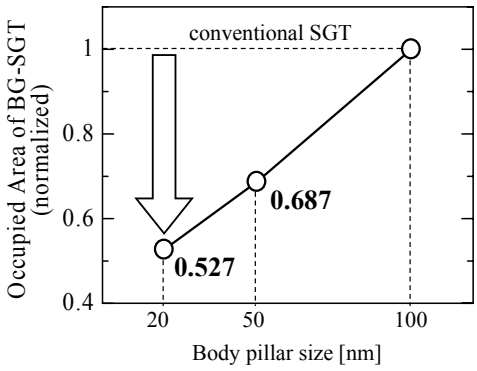

Fig.5 Dependence of occupied area on body pillar size of BG-SGT

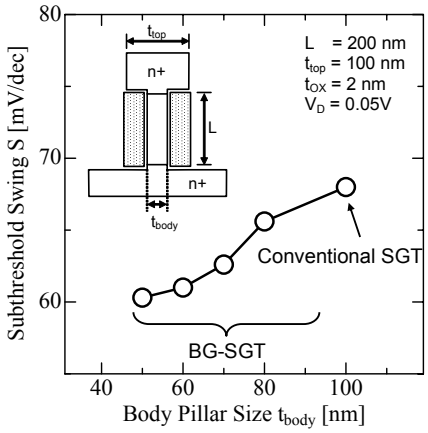

Fig.6 Dependence of subthreshold swing S on body pillar size for conventional SGT and BG-SGT

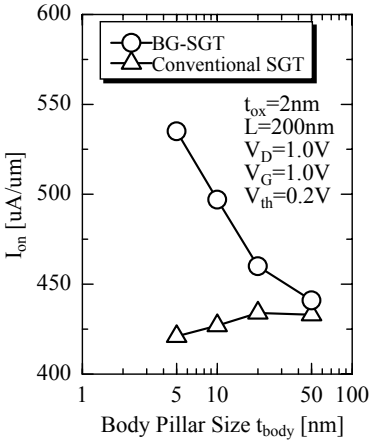

Fig.7 Dependence of drive current on body pillar size for conventional SGT and BG-SGT

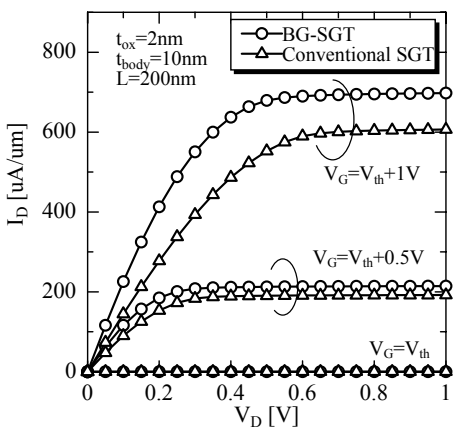

Fig.8 I_D-V_D characteristics of conventional SGT and BG-SGT