Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 632-633

P9-7

Thermal conductivity of high-integrity nanometer buried oxides by SIMOX

Yemin Dong[1], Xiang Wang[1], Jing Chen[1], Meng Chen[1,2], Xi Wang[1,2],
Ping He[3], Lilin Tian[3] and Zhijian Li[3]

[1]Ion Beam Laboratory, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, 865 Changning Road, Shanghai 200050, China
Phone: +86-21-6251-1070; E-mail: acrodym@yahoo.com
[2]Shanghai Simgui Technology Co., Ltd., 200 Puhui Road, Jiading, Shanghai 201821, China
[3]Institute of Microelectronics, Tsinghua University, Beijing 100084, China

1. Introduction

With the feature length scaling down into nanometer regime, the self-heating effect becomes more and more important in SOI circuits due to the very low thermal conductivity of buried oxide layer (BOX). An accurate value of the thermal conductivity of BOX, especially nanometer BOX, is essential for predicting the self-heating effect of SOI circuits. However, up to now, very few data are available for BOX used in SOI technology [1]. In this work, high-integrity nanometer BOX layers were fabricated by SIMOX technique and thermal conductivity of these very thin BOX layers were measured by a modified method presented by Tenbroek [2].

2. Fabrication of nanometer BOX

Oxygen ions were implanted into 100 mm *p*-type (100) wafers with doses of 2.5~4.8×10^{17} cm^{-2} at energies of 70~140 keV [3]. After implantation, the samples were subsequently annealed at 1300 °C for 5 h in an Ar+O_2 (<3%) ambient. The quality of BOX was detected by cross-sectional transmission electron microscopy (XTEM). Fig. 1 shows the XTEM micrographs of wafers implanted with 2.5, 3.5, 4.5, and 4.8×$10^{17}$$cm^{-2}$, at optimized energy of 70, 100, 130, and 140 keV, respectively. The thicknesses of BOX layers are 55, 70, 83, and 90 nm, respectively. It is clear that the BOX layers are continuous and contain no silicon islands. These high-integrity BOX layers result from the optimization of oxygen ion dose and energy [3]. High integrity of BOX layers in this work guarantees the accurate measurement of thermal conductivity because the influences of silicon pipes or silicon islands in BOX layers are minimized.

3. Measurement of thermal conductivity

As in the method of Tenbroek *et al.* [2], a four-terminal resistor, shown in Fig. 2, was fabricated in the top silicon layer over the BOX layer using the CMOS process. The structure is used both as the heater and thermometer. A large bias current I_B is applied to the A and D end points and the resulting difference in voltage between B and C, V_M, is measured. Thus, the power dissipated in this region and electrical resistance can calculate to be $P=V_M I_B$, and $R_{el}=V_M/I_B$. First, the wafer temperature is set to T_{ambi1} using a heated chuck and I_B-V_M characteristics of the resistors are measured. Then the wafer temperature is changed to T_{ambi2} and the large current I_B-V_M is measured again. Successively calculated R_{el} vs P curves are plotted for each temperature, shown in Fig. 3. Supposed that R_{el} is the same for the same working temperature, thus the total thermal resistance of the active region can be obtained:

$$R_{th,\,tot} = -\Delta T_{ambi}/\Delta P \qquad (1)$$

Taking the substrate thermal resistance and other path of heat flowing away into account, the total thermal conductance of the active region can be modeled as

$$\Theta = \Theta_0 + \left(\frac{W \ln \frac{3L}{W}}{3\lambda_{Si}} + \frac{t_{BOX}}{\lambda_{BOX,eff}} \right)^{-1} WL, \qquad (2)$$

where Θ_0 represents all heat flow from the resistor sideways and dose not depend on the width of the main resistor, t_{BOX} is the thickness of the BOX layer, W and L are the width and length of the active region, respectively, λ_{Si} is the thermal conductivity of the silicon, and $\lambda_{BOX,eff}$ is the effective

thermal conductivity of the BOX. To determine the $\lambda_{BOX,eff}$, a series of resistor with different widths are made on the same die and the thermal conductance for each active region is measured using the above method. The $\lambda_{BOX,eff}$ are determined using nonlinear curve fitting as shown Fig. 4.

Fig. 5 illustrates the thermal resistance of the BOX layers per unit area R_{th} with different thicknesses, together with the result from reference [2]. Suppose that

$$R_{th} = t_{BOX}/\lambda_{BOX,eff} = R_{th,bd} + t_{BOX}/\lambda_{BOX,int}, \qquad (3)$$

Where $R_{th,bd}$ is the boundary resistance per unit area of Si-SiO_2 interfaces and the $\lambda_{BOX,int}$ is the internal thermal conductivity the BOX. The values of $R_{th,bd}$ and $\lambda_{BOX,int}$ are obtained by curve fitting and the results are 6.5×10^{-8} m^2KW^{-1} and 0.94 $Wm^{-1}K^{-1}$, respectively. It is obvious that the linearity of the R_{th} dependence on t_{BOX} is very good and assures the accuracy of the values of $R_{th,bd}$ and $\lambda_{BOX,int}$ determined.

4.Conclusions

In summary, accurate measurement of thermal conductivity of high-integrity nanometer BOX layers was performed. The thermal conductivity of nanometer BOX layers not less than 55 nm does not depend on the BOX thickness and is less than the fused bulk silica value of 1.4 $Wm^{-1}K^{-1}$. Furthermore, quit large boundary thermal resistance between Si-SiO_2 interfaces is found that cannot be neglected in SIMOX SOI circuits.

References

[1] K. E. Goodson, M. I. Flik, et al., IEEE Electron Device Lett. 14, 490 (1993)

[2] B. M. Tenbroek, R. T. Bunyan, et al., IEEE Trans. Electron Devices 46, 251 (1999)

[3] M. Chen, X. Wang, et al., Appl. Phys. Lett. 80, 880 (2002)

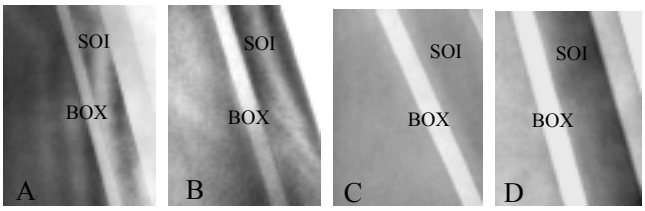

Fig. 1 XTEM micrographs of wafers implanted with $2.5\times10^{17}cm^{-2}$ at 70 keV (A), $3.5\times10^{17}cm^{-2}$ at 100 keV (B), $4.5\times10^{17}cm^{-2}$ at 130 keV (C), $4.8\times10^{17}cm^{-2}$ at 140 keV (D).

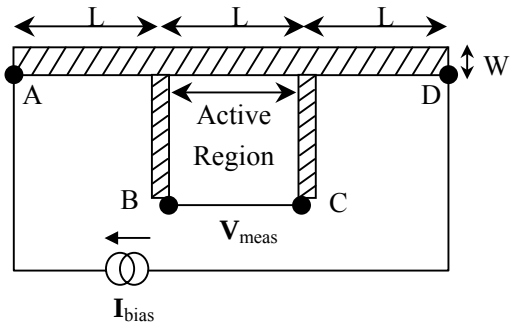

Fig. 2 Layout of the four-terminal resistor

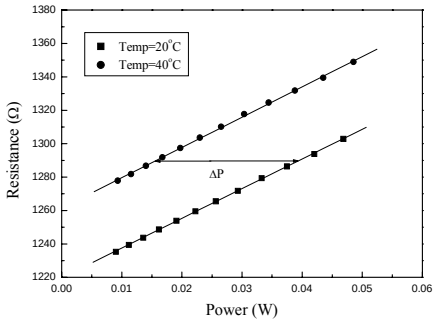

Fig. 3 Measured electrical resistance with increased power dissipation. The thickness of BOX is 90 nm.

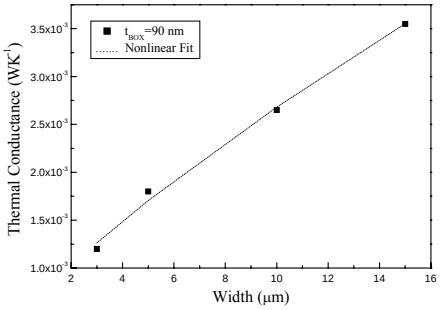

Fig. 4 Measured total thermal conductance with different widths and the nonlinear fitting result.

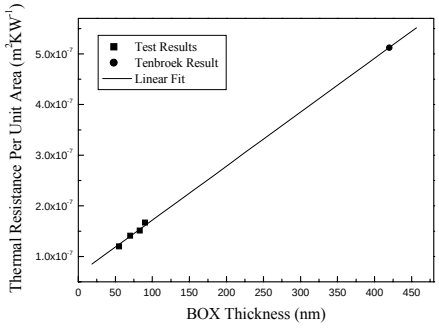

Fig. 5 Measured thermal resistance per unit area of the BOX layers with different BOX thicknesses.