Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 636-637

P9-9L

Patterned SIMOX SOI materials with high degree of surface planarity and low defect density

Yemin Dong[1], Xi Wang[1,2], Meng Chen[1,2], Jing Chen[1], Xiang Wang[1,3], Wanbing Yi[1,3], Bo Jin[1] and Enxia Zhang[1]

[1]Ion Beam Laboratory, Shanghai Institute of Microsystem and Information Technology (SIMIT), Chinese Academy of Sciences (CAS), 865 Changning Road, Shanghai 200050, China
Phone: +86-21-6251-1070; E-mail: acrodym@yahoo.com
[2]Shanghai Simgui Technology Co., Ltd., 200 Puhui Road, Jiading, Shanghai 201821, China
[3]TD Unit, Grate Semiconductor Manufacturing Corporation, Shanghai 201203, China

1. Introduction

In recent years, the SOI technology has started to be used as the mainstream technology in CMOS LSIs to maintain the performance gain according to the Moore's law. Although RF/analog LSIs, DRAMs, imagers and so on have been demonstrated on the SOI substrates recently, there are some challenges in fabricating these circuits on SOI, particularly DRAMs on SOI substrate [1]. Patterned SOI technology [2,3] is a realistic method to integrate RF/analog circuits, DRAMs, imagers, which are fabricated over bulk silicon regions, together with high-speed and low-power logic circuits that built over SOI regions. Therefore, use of patterned SOI substrate for system-on-a-chip integration will help circumambulate the constraint and widen the degree of freedom in design and fabrication.

In addition, patterned SOI technology is also attractive for fabrication of a novel DSOI (drain and source on insulator) MOSFET, where the drain and source regions were positioned on the patterned buried oxide layers while the channel region is left connected to the substrate to eliminate the floating-body and self-heating effects of SOI devices [4].

SIMOX is one of the most promising techniques for fabricating patterned SOI materials because of its simplicity, maturity and compatibility with silicon LSIs manufacturing processes [5-7]. However, it is very difficult to obtain high quality patterned SOI materials due to the formation of patterned BOX layers in silicon wafers by high-dose oxygen implantation. In the present work, an effort was made to fabricate high quality patterned SOI wafers by masked low-dose and low-energy SIMOX technique.

2. Experiment

The starting materials were 100 mm *p*-type (100) CZ silicon wafers. A thermal oxide of 500 nm was firstly grown and structured as mask by reactive ion etching. $^{16}O^{+}$ were implanted into the masked wafers with doses of 2.0 and 3.5×10^{17} cm^{-2} at optimized energies of 50 and 100 keV, respectively [8]. During the ion implantation, the wafer temperature was kept at 680 °C. After etching out mask by diluted HF, the sample was subsequently annealed at 1300 °C for 5 h in argon ambient with oxygen less than 3%.

3. Results and discussion

Fig. 1 shows XTEM micrograph of the annealed wafer subjected to an oxygen dose of 2.0×10^{17} cm^{-2} at ion energy of 50 keV. It is clear that the patterned SOI region contains a superficial silicon layer and a continuous BOX layer. Thicknesses of the superficial silicon layer and the BOX layer were 57 and 49 nm, respectively. No silicon islands were observed in the BOX layer, indicating a BOX layer of high integrity. The result revealed that the low-dose SIMOX process was not at the expense of the integrity of the BOX layer. In addition, the XTEM micrograph did not reveal the presence of any structural defect around the BOX edge. This indicates the defect density lower than 10^5 cm^{-2}, the detection limit of the TEM. However, in the case of high-dose patterned SOI materials [5,6], the defect density was very high (~10^8 cm^{-2}) and the defects extended out of the BOX edge about 2~3 micrometers [5].

Fig. 1 also illustrates that the surface from the SOI to bulk silicon regions was exceptionally flat with no height step between the silicon surfaces in the SOI region and the bulk region. The planarity is much superior to that of the high-dose patterned SOI materials. Bentum *et al.* [5] reported that the height difference between the SOI and bulk silicon regions of the annealed sample implanted with conventional high-dose of 1.8×10^{18} cm^{-2} was approximately 180 nm. The wafers with such a large height step is obviously not applicable to advanced lithography, especially in deep-submicron and nanometer regime. However, with

current approach, this obstacle for wide adoption of patterned SOI technology is surmounted.

Fig. 2 shows a typical XTEM micrograph of the patterned SOI material with deep-submicon spacing BOX layers after oxygen ions implantation with a dose of 3.5×10^{17} cm^{-2} at 100 keV and high temperature annealing. Similar to Fig. 1, the BOX layers were high integrity without any detectable silicon islands or pipes, and the surface was very planar. Moreover, the transitions between the patterned BOX layers and the bulk silicon around are abrupt and contain no detectable structural defects therein. The spacing between the two buried oxides is only 210 nm, which ensures the deep-submicron DSOI device fabrication.

During the formation of the BOX layers one unit volume of silicon converts into 2.25 unit volumes of SiO_2. It is this large expansion that resulted in large height steps observed in high-dose patterned SOI. Moreover, the dislocation generation around the BOX edges is also believed to be a result of the large stress induced due to the same volume expansion of the local BOX formation [5]. Therefore, reducing the implanted oxygen dose to form very thin BOX layers is a feasible approach to improve the patterned SOI quality. Because of very low dose oxygen implantation (2.0 and 3.5×10^{17} cm^{-2}), the swelling due to the BOX formation was small and consequently the quality of the materials was improved. Furthermore, compared with high-dose SIMOX, in low-dose SIMOX case, no stoichiometric BOX layers were formed before high-temperature annealing. During the internal oxidation of the implanted oxygen, silicon atoms were ejaculated into the matrix and became self-interstitials to provide necessary space for BOX layers formation [9]. These generated silicon interstitials migrated to the surface through the bulk silicon region and epitaxially grew on the surface. Therefore, the surface of the low-dose patterned SOI material was remarkably planar.

4. Conclusion

In summary, masked low-dose and low-energy SIMOX is an elegant method for fabrication of patterned SOI materials with quality superior to those prepared by conventional techniques. The patterned SOI materials prepared with such masked SIMOX technique exhibit high quality featured by low-density-defect transition of SOI and bulk silicon region and high degree of surface planarity. The formed patterned SOI materials are very attractive for SOC and novel DSOI MOSFET applications.

References

[1] M. Yoshimi, Solid-State Electron. 46, p.651 (2002).

[2] H.L. Ho, et al., IEDM Tech. Dig., p.474 (2001).

[3] A. Ogura, IEEE Int. SOI Conf. Proc., p.185 (2002).

[4] P. He, X. Lin, et al., IEEE Int. SOI Conf. Proc., p.55 (2002).

[5] R.V. Bentum, H. Vogt. IEEE Int. SOI Conf. Proc., p.49 (1998).

[6] S. Bagchi, et al., IEEE Int. SOI Conf. Proc., p.121 (1999).

[7] A. Ogura, Appl. Phys. Lett. 82, p.4480 (2003).

[8] M. Chen, X. Wang, et al., Appl. Phys. Lett. 80, p.880 (2002).

[9] J. Margail, et al., Appl. Phys. Lett. 54, p.526 (1989).

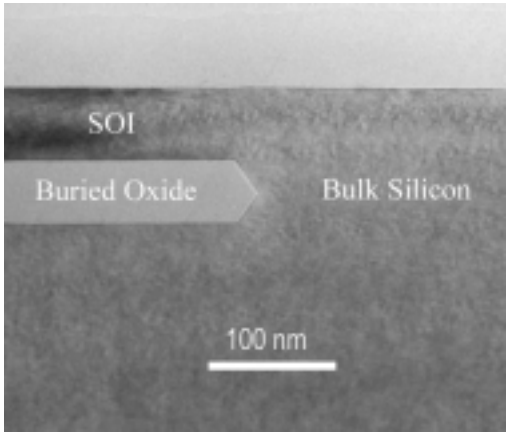

Fig. 1 XTEM micrograph of the patterned SOI material implanted with $2.5\times10^{17}cm^{-2}$ at 50 keV.

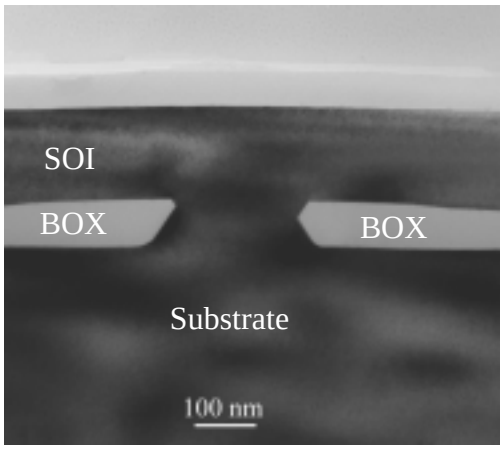

Fig. 2 XTEM micrograph of the patterned SOI material with deep-submicon spacing BOX layers for novel DSOI MOSFET application.