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Gate Stress Induced Performance Enhancements

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1. Introduction

Localized strain is considered an excellent candidate for performance enhancement due to its superior scaling with smaller gate lengths [1,2]. It can be achieved by uniaxial straining from source and drain [3], from deposited over-layers [1,4], or from various 3-d films with intrinsic stress [5,6]. Gate itself can be a very effective source of channel straining and its effects are less understood. In the past stress induced by the gate polycide was considered a reliability problem [7]. In this paper we present experimental data from 20nm extremely thin SOI (ETSOI) devices and 35nm bulk and biaxially strained devices with metal gates and 3-d computer simulations to show implementation of stress in the gate itself for enhancing performance of fully depleted devices.

2. Stress Transfer

Stress tensor has three major components: longitudinal, transverse, and vertical. There is a huge difference how different straining approaches transfer stress into the channel for all components [8]. Fig.1 shows stress transfer efficiency of intrinsic stress in metal gate, over-layer and high κ film for planar devices and FinFETs. While the absolute amount of stress transfer depends on device geometry, the trend should be valid for geometries that are going to be applied for the 45 and 32nm technology node. Different position of the gate in reference to the direction of current flow causes different stress transfer. A gate with tensile built-in stress would cause compressive longitudinal stress in the channel for planar devices, but for FinFETs it would induce tensile stress. A tensile transverse stress benefits both NMOS and PMOS [5], while compressive vertical component is beneficial for NMOS and tensile for PMOS. For planar devices compressive built-in stress in the gate will enhance NMOS, while for FinFETs a tensile gate is a better choice for NMOS. Unfortunately, PMOS requires the opposite type of stress in the gate.

3. Gate Stress for Fully Depleted Devices

Gate stress engineering for three major types of fully depleted devices (single-gate ETSOI, tri-gate, and FinFET) is different. Wide ETSOI devices behave like regular planar devices and results from Fig. 1 can be applied. A very different behavior was observed for narrow ETSOI devices [6]. The huge difference in linear transconductance (Fig. 2) can be explained by applying the stress transfer theory. For wide devices the tensile stress in the Ni-rich fully silicided (FUSI) gate induces compressive longitudinal stress in the channel, thus degrading NMOS devices. For narrow devices with mesa isolation there are two gates on the sidewall and from Fig. 1 we see that they induce tensile longitudinal stress. The narrower the device the more beneficial the side gates are, which results in increasing I_{on} for narrow devices. The 3-d computer simulations show that for narrow NMOS ETSOI devices compressive stress shows larger I_{on} enhancement (Fig. 3), as expected from the stress transfer theory. The thinner silicon channel improves NMOS devices with tensile gates (Fig. 4) and degrades those with compressive gates. High R_{sd} usually obscures this effect. Fig. 5 shows large signal transconductance for ETSOI devices with tensile gates. Larger R_{sd} for 4.5nm thick channel causes lower transconductance. The balance of stress transfer is critical for designing high-performance tri-gate devices. There is always an interaction of gate stress with other sources of stress, which requires a thorough optimization. For FinFET devices the fin height diminishes I_{on} enhancement (Fig. 6), which is undesirable from the area efficiency point of view. Straining through the gate by using over-layers with built-in stress require thick films and tall gates [1,2], which goes against scaling trends. While for planar devices the thickness of the gate electrode affects I_{on} by 1%/10nm, for FinFETs and tri-gates the gate thickness is not critical, because side gates affect strain differently than the top gate (Fig. 7) At the 45nm node it is anticipated that high κ gate dielectrics will be introduced. We expect that those films will have some built-in stress. Fig. 8 shows how high κ stress affects FinFET devices for different dielectric thicknesses.

4. Gate Stress in Bulk and Biaxially Strained Devices

In narrow bulk devices built-in stress in the gate interacts with stress from the shallow trench insulation and with a biaxial strain from the SiGe layer for strained silicon devices. The compressive stress in the NiSi (FUSI) gate [9] improves NMOS linear transconductance by 46% for 35nm long and 250nm wide transistors (Fig. 9) and PMOS linear transconductance by 60% compared to poly gates (Fig. 10). In the case of strained silicon from 20% Ge content layer NMOS increases only 6% and PMOS decreases by 38% compared to poly gates. If we compare FUSI gates for strained and unstrained cases we see slight degradation for strained NMOS devices and severe degradation for strained PMOS devices. Strained NMOS devices have larger I_{off} than regular bulk devices. Strained PMOS devices have large leakage current, strain lower threshold voltage by 170mV for poly devices but only by 40mV for FUSI devices. Gate stress drastically reduces R_{on}, shown in Figs. 11 and 12 for NMOS and PMOS devices, respectively. In both cases an addition of biaxial strain from the SiGe layer to the metal gate degrades transistor output characteristics.

5. Conclusions

We show examples of gate stress on fully depleted, bulk, and strained silicon devices. A simple stress transfer theory can explain trends in device performance. Interactions between different sources of strain and the true three-dimensional nature make accurate predictions difficult. For high performance technologies two gate electrodes with opposite built-in stress will be needed to maximize performance enhancement for both NMOS and PMOS devices. FUSI gates represent an excellent choice for introducing gate stress since it is the last high temperature step in the process, thus minimizing strain relaxation. Built-in stress in the gate offers larger enhancements than the one that can be achieved in currently used stressed over-layers.

References

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[2] M.D. Giles et al, VLSI Symp. 2004, p.118
[3] T. Ghani et al, *IEDM 2003*, p.978
[4] F. Ootsuka et al, *IEDM 2000*, p.575
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[7] A. Hamada and E. Takeda, *VLSI Symp. 1992*, p.98
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[9] Q. Xiang et al, VLSI Symp. 2003, p.101

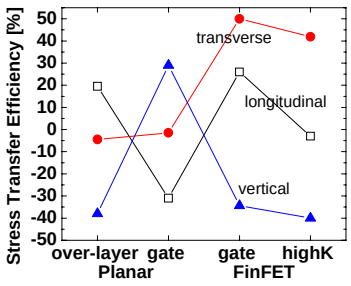

Fig. 1: Stress transfer efficiency for planar and FinFET devices. Negative numbers represent opposite type of stress.

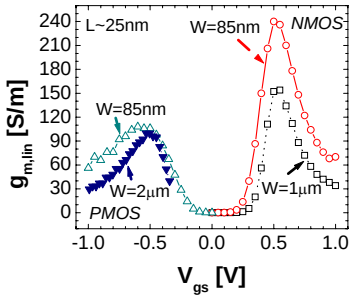

Fig. 2: Linear transconductance for narrow and wide ETSOI devices (from Ref. 6).

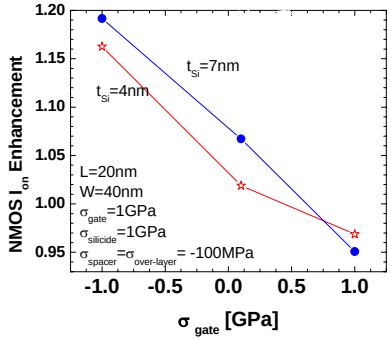

Fig. 3: Simulated NMOS drive current enhancement for different gate stress.

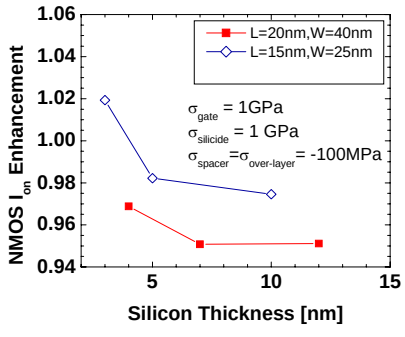

Fig. 4: Gate stress effect on NMOS drive current vs. silicon channel thickness (simulations).

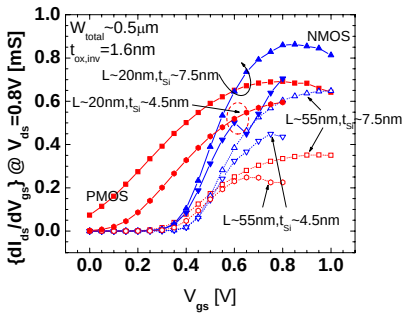

Fig. 5: Saturation transconductance for narrow ETSOI devices with different silicon thickness.

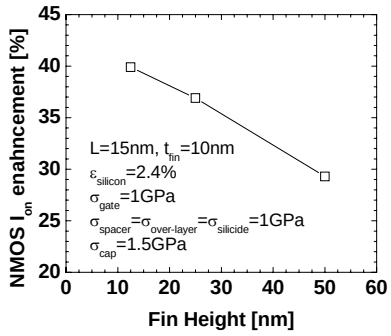

Fig. 6: FinFET NMOS drive current enahancement vs. fin height.

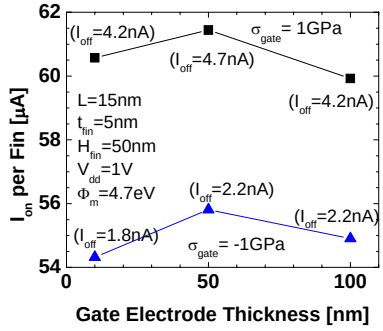

Fig.7: Simulated FinFET NMOS drive currents vs. gate thickness.

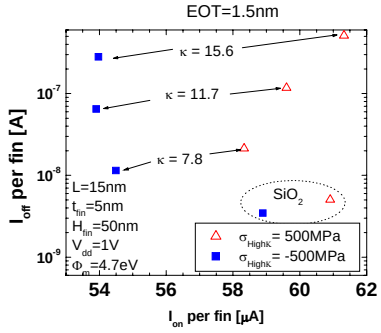

Fig. 8: Effect of stress in high κ layer on NMOS FinFETs (simulations).

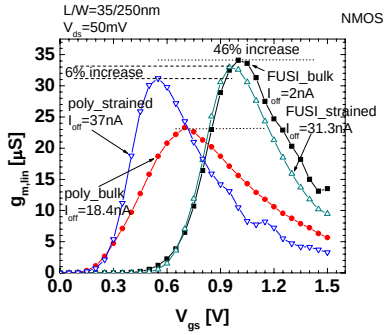

Fig. 9: Linear transconductance of 35nm strained and bulk FUSI and poly NMOS devices.

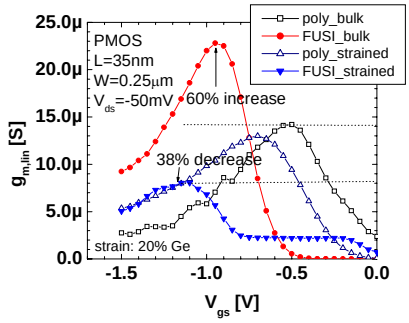

Fig. 10: Linear transconductance of 35nm strained and bulk FUSI and poly PMOS devices.

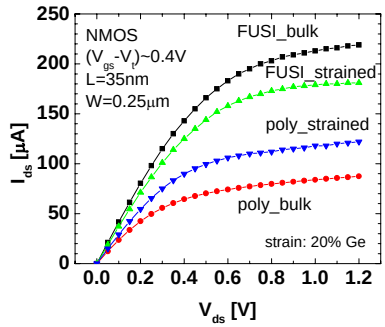

Fig. 11: Output characteristics for 35nm strained and bulk FUSI and poly NMOS devices.

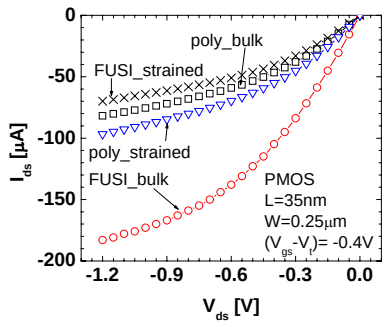

Fig. 12: Output characteristics for 35nm strained and bulk FUSI and poly PMOS devices.