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Physical Origin of Drive Current Enhancement in Ultra-thin Ge-On-Insulator (GOI) MOSFETs under Full Ballistic Transport

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1. Introduction

It is expected for MOSFETs with ultra-short L_g around or less than 10 nm that carriers are dominated by ballistic or quasi ballistic transport with few scattering events inside channels. Under full ballistic transport regime, the current drive of MOSFETs is determined by the product of injection carrier velocity at the source edge, v_{inj}, and surface carrier concentration, N_s, suggesting that the increase in v_{inj} is important for further improving the drive current of ballistic MOSFETs. Therefore, I have proposed a scenario of injection velocity engineering by the optimum choice and modulation of the subband structures in MOS inversion layers, where one of promising device structures is ultra-thin GOI (Ge-On-Insulator) MOSFETs [1].

However, physical mechanisms determining the drive current of GOI MOSFETs have not been clearly understood yet. Also, while it has recently been pointed out that the electrical properties of GOI MOSFETs with ultra-short L_g are strongly dependent on the surface orientations [2, 3], the surface orientation optimized in terms of device performance of ballistic GOI MOSFETs has not been fully identified yet. Thus, this paper examines the physical origin of the current drive enhancement of thin body ballistic GOI n-channel MOSFET, its GOI thickness (T_{GOI}) dependence and its surface orientation dependence, through theoretical calculations, by discriminating the effects of v_{inj} and N_s on the drive current.

2. Physical Parameters Related to Drive Current

A simple and analytical model of drain saturation current in n-MOSFET, I_{sat}, under ballistic transport, formulated by Natori [4], is used in this study for qualitatively analyzing the drive current. As seen in Fig. 1, the calculated v_{inj} for 2-fold valleys of (100) Si suggests that lower effective mass (m^*) parallel to the channel direction and lower density-of-states (DOS) (lower m^* and lower valley degeneracy) are effective in increasing v_{inj} [1]. Table 1 shows the effective mass and the valley degeneracy of Si and Ge inversion-layer electrons on each surface orientation. According to the above guideline, Ge (111), particularly, the first subband ladder can be the optimum electronic system, in terms of obtaining high v_{inj}. On the other hand, I_{sat} is also dependent on N_s, which is affected by inversion-layer capacitance, C_{inv}, as also shown in Table 1. Smaller C_{inv} leads to lower C_g and resulting lower N_s at a given V_g value, leading to lower I_{sat}. Since, as shown later, the modulation of the subband structure due to changing surface orientations or thinning T_{GOI} [1] can provide the opposite influences on v_{inj} and C_{inv}, the impact of the subband structures needs to be analyzed for v_{inj} and C_{inv}, separately. Here, v_{inj}, C_{inv} and I_{sat} are calculated from electron subband energies and occupancies of 7 and 5 subbands for the first and the second ladder, respectively, which are determined by Poisson-Schrodinger self-consistent calculations. The current flow direction is taken to be parallel to <110>, yielding the largest drive current on each surface orientation.

3. Results

Fig. 2 shows calculated v_{inj} of (111) GOI MOSFETs as a function of T_{GOI} at a fixed value of N_s, confirming that v_{inj} increases with a decrease in T_{GOI}. This enhancement is attributed to the preferential increase in the subband energy of the higher ladders, associated with thinning T_{GOI}, and the resulting increase in the occupancy in the lower ladder on (111), having lower m^* and higher v_{inj}. However, it is found in Fig. 3 that the increase in v_{inj} is not observed for (100), while (110) has a moderate T_{GOI} dependence. This dependence of v_{inj} on (100) is explained by the fact that the (100) has only one ladder and, thus, has no change in the occupancy with thinning T_{GOI}. These interpretations are confirmed by comparing v_{inj} of each subband in higher and lower ladders on (100), (110) and (111) surfaces. It is also found that v_{inj} in thin T_{GOI} is largest for (111) and decreases, according to the order of (111), (110) and (100).

On the other hand, the amount and the T_{GOI} dependence of C_{inv} are opposite to those of v_{inj}. Fig. 4 shows the calculated C_{inv} and inversion-layer thickness ($T_{inv} = \varepsilon_{Ge}/Z_{av}$) as a function of T_{GOI}. C_{inv} on (100) significantly increases with decreasing T_{GOI}, attributed to the decrease in T_{inv}, caused by the decrease in the physical thickness of GOI films [5]. In contrast, it is found that C_{inv} on (111) gradually decreases with decreasing T_{GOI}, attributed to the dominant contribution of lower DOS on C_{inv}. It has been reported [6] that C_{inv} is composed of the component due to DOS and that due to a finite value of T_{inv}. It is confirmed from the comparison of total C_{inv} with C_{inv} due to DOS in Fig. 5 that, in very thin T_{GOI}, C_{inv} on (111) is perfectly dominated by DOS, because of much lower value of DOS on (111) than on (100). As a result, in T_{GOI} less than 10 nm, N_s on (111) at a given V_g value slightly decreases, as seen in Fig. 6, because the effect of lower DOS compensates or surpasses that of the decrease in T_{inv}. On the other hand, N_s on (100) increases with a decrease in T_{GOI}, simply attributed to the decrease in T_{inv}. This N_s increase directly leads to the enhancement of I_{sat}. C_{inv} and N_s on (110) have intermediate characteristics between (100) and (111).

To what degree the effect of C_{inv} contributes to I_{sat} is strongly dependent on equvallent gate insulator thickness, T_{eq}. As a result, the optimum surface orientation also depends on T_{eq}. In the limit of thin T_{eq} (= 0 nm), as seen in Fig. 7, I_{sat} of ultrathin T_{GOI} at a given V_g is largest for (100) and (110), while I_{sat} is largest for (111) and (110) in T_{eq} of 1 nm. Also, I_{sat} of thick GOI or bulk Ge MOSFET is the largest for (111) and (110), irrespective of T_{eq}. These results suggest that (110) could be the optimum orientation. However, one drawback of (110) is the strong anisotropy in I_{sat} (Fig. 8), attributed to the anisotropic effective mass, making the CMOS layout design quite complicated. Thus, an appropriate choice of (111) and (100) surfaces, depending on T_{eq} and T_{GOI}, can be a reasonable solution for optimum device design of GOI MOSFET.

4. Conclusion

It was found that the physical origin of the drive current enhancement in GOI n-MOSFET with decreasing T_{GOI} is different between (111) and (100), ascribed to the increase in v_{inj} for (111) and the increase in C_{inv} for (100).

References [1] S. Takagi, VLSI Symp. (2003) 115 [2] A. Rahman et al., IEDM (2003) 471 [3] T. Low et al., IEDM (2003) 691 [4] K. Natori, IEICE Trans. Electron., E84-C (2001) 1029 [5] S. Takagi, IEICE Trans. Electron., E85-C (2002) 1064 [6] S. Takagi et al., TED-42 (1995) 2125

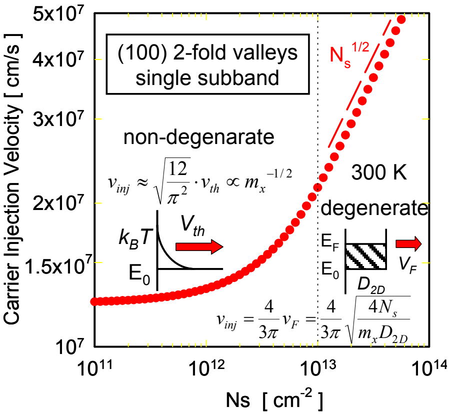
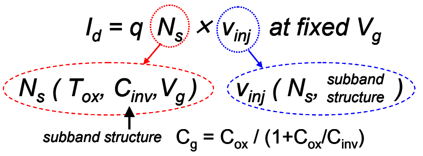


Fig.1 Calculated injection velocity of Si 2-fold valleys on (100) as a function of N_s



unit: m0	surface orientation	channel direction	1st ladder			2nd ladder		
			mx	my	Mv	mx	my	Mv
Si	(100)	<011>	0.19	0.19	2	0.19	0.916	2
						0.916	0.19	2
	(110)	<001>	0.19	0.553	4	0.916	0.19	2
		<110>	0.553	0.19	4	0.19	0.916	2
	(111)	<110>	0.412	0.232	4			
			0.19	0.674	2			
Ge	(100)	<011>	0.082	1.12	2			
			1.12	0.082	2			
	(110)	<001>	0.601	0.082	2	0.12	0.224	2
		<110>	0.082	0.601	2	0.224	0.12	2
	(111)	<110>	0.082	0.082	1	0.082	1.467	1
						0.281	0.107	2

Table 1 Effective mass and the valley degeneracy of Si and Ge inversion-layer electrons on each surface orientation

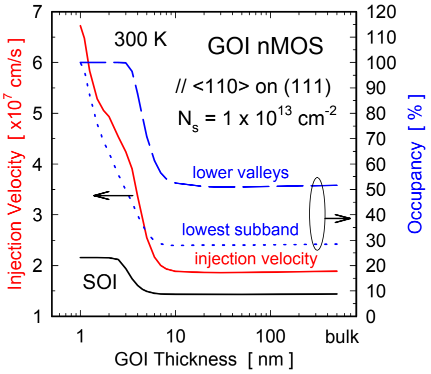


Fig. 2 Calculated v_{inj} of (111) GOI n-MOSFETs as a function of T_{GOI} at a fixed N_s value of 1×10^{13} cm^{-2}

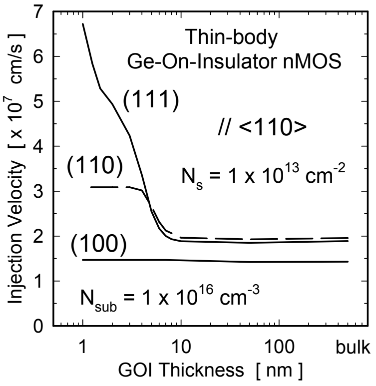


Fig. 3 Calculated v_{inj} of (100), (110) and (111) GOI n-MOSFETs as a function of T_{GOI} at N_s of 1×10^{13} cm^{-2}

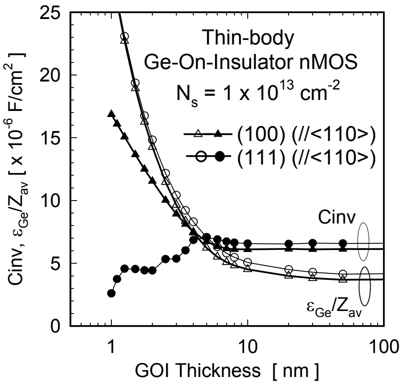


Fig. 4 Calculated C_{inv} and T_{inv} of (100) and (111) GOI as a function of T_{GOI} at N_s of 1×10^{13} cm^{-2}

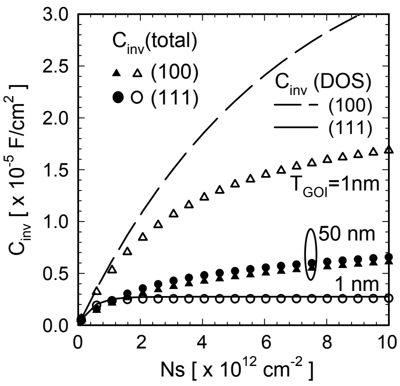


Fig. 5 Calculated total C_{inv} and C_{inv} due to DOS for (100) and (111) GOI with T_{GOI} of 50 nm and 1 nm as a function of N_s

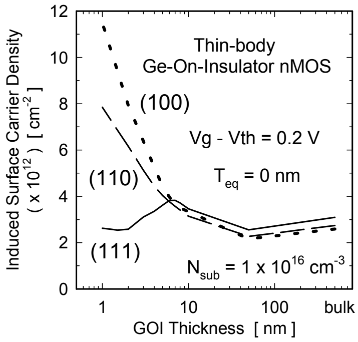


Fig. 6 Calculated N_s on (100), (110) and (111) GOI at V_g-V_{th} of 0.2 V as a function of T_{GOI}

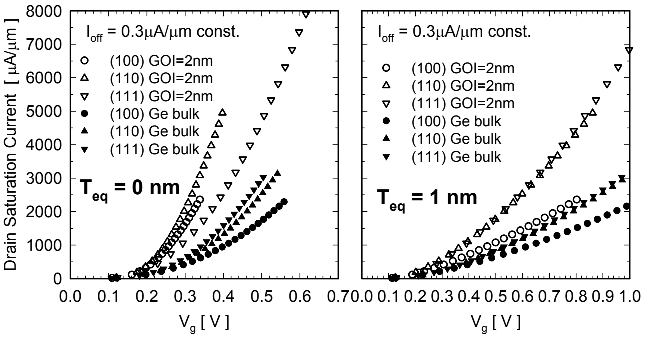


Fig. 7 Calculated I_{sat} - V_g characteristics of (100), (110) and (111) GOI (T_{GOI} of 2 nm) and bulk Ge n-MOSFET with T_{eq} of 0 nm and 1 nm at a fixed I_{off} value of 0.3 μm/μA

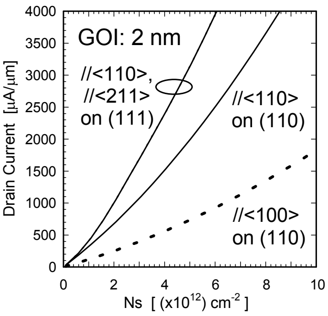


Fig. 8 Channel direction dependence of I_{sat} on (110) and (111) GOI with T_{GOI} of 2 nm