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Suppression of Boron Penetration from S/D Extension to improve Gate Leakage Characteristics and Gate-Oxide Reliability for 65nm node CMOS and beyond

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1. Abstract

Boron penetration occurs not only from doped gate poly-silicon but also from substrate, and brings several degradations on gate-oxide characteristics [1, 2]. On the other hand, boron concentration of S/D-extension has been increasing according to pMOS gate scaling. We found that boron penetration from the S/D-extension becomes crucial issue on gate leakage and gate-oxide integrity, especially for deep sub-micron pMOS [3]. In this paper, we study several treatments in detail to suppress boron penetration from the S/D-extension, and demonstrate the plasma nitridation treatment after gate etching is the best solution for 65nm CMOS and beyond.

2. Introduction

Nitridation technique of the gate-oxide top surface has been much studied to suppress the boron penetration from the doped gate poly-silicon and proved to be efficient against NBTI degradation [4]. However there is another path for boron to penetrate to gate-oxide from the substrate, where this technique is helpless. Fig. 1 shows the boron penetrating model from S/D-extension which we suppose for the present. We investigate some phenomena caused by boron penetration from S/D-extension, and demonstrate that nitridation after gate etching is very efficient to control this new degradation mode. We also propose optimized nitridation method after gate etching.

3. Gate Leakage Current and TDDB in pMOS

Fig. 2 shows the dependence of inversion gate leakage current on gate length for MOSFETs fabricated by the conventional process with SiON thin-film. At longer gate, the leakage current of pMOS is much smaller than that of nMOS. While leakage current of nMOS decreases almost linearly with gate length, leakage current of pMOS seems to saturate at gate length below 0.1 μm. Due to this edge effect, gate leakage current of short channel pMOSFET is comparable to or larger than that of nMOSFET. This phenomenon has quite a large impact on the setting of gate-oxide thickness, since gate leakage current of nMOSFET has been considered to determine the off-current limit. The gate leakage current of pMOSFETs is also found to deteriorate in proportion to boron concentration of S/D-extension, as shown in Fig. 3.

The edge effect of pMOSFET also appears on the gate oxide integrity. Fig. 4 shows the TDDB characteristics of flat capacitors and array-transistors, where failure probabilities are normalized to defect density since they have different sizes. The results for nMOS flat capacitors and array-transistors are consistent. For pMOS, however, array-transistors show apparent deterioration. The degradation of gate-oxide of array-transistors is considered to originate from boron diffusion from S/D-extension.

4. Solution for Boron penetration from S/D Extension

Fig. 5 shows the gate leakage current by two types of gate dielectrics. One is SiON thin-film by plasma nitridation on base silicon oxide, and the other is SiON thin-film by NO/O_2 oxi-nitridation. The gate leakage current of SiON thin-film by plasma nitridation is larger than that of SiON thin-film by NO/O_2 oxi-nitridation. Fig. 6 shows the nitrogen profile of these two types of SiON thin-film. While the nitrogen peak is close to gate electrode for SiON thin-film by plasma nitridation, the nitrogen peak is on the boundary between gate dielectrics and silicon substrate for SiON thin-film by NO/O_2 oxi-nitridation. The gate dielectrics formed by NO/O_2 can not be adopted because of NBTI degradation, though these results indicate that nitrogen near S/D-extension suppresses boron penetration from S/D-extension. Fig. 7 shows the boron-suppressed model from S/D-extension in case of SiON thin-film by NO/O_2 oxi-nitridation.

In consideration of these results, such a nitrogen profile as Fig.8 is supported to suppress not only NBTI degradation but also boron penetration from both gate electrode and S/D-extension. To realize this structure, we investigated the treatment after gate etching. We prepared samples with three types of treatments; plasma nitridation treatment after gate etching, NO/O_2 treatment after gate etching and only oxide offset deposition without nitridation. Fig. 9 shows the gate length dependence of normalized gate leakage current in these samples. The gate leakage current is suppressed with both of nitride treatments. Fig.10 shows the nMOS drive current versus the pMOS drive current in these samples. The sample treated by plasma nitridation is the best for nMOS drivability. For the sample treated by NO/O_2, nMOS driverability has deteriorated. This nMOS degradation is supposed from the parasitic resistance by reduced overlap between S/D-extension and gate electrode. That is, NO/O_2 treatment is not so strong in nitridaion ability that the offset spacer fabricated during NO/O_2 treatment becomes thick when NO/O_2 treatment is strengthened to get efficient boron suppressed effect.

Fig. 11 shows the dependence of T_{BD} distributions of pMOS transistors with and without plasma nitridation after gate etching. The sample with plasma nitridation is better than that without plasma nitridation. Fig. 12 shows pMOS current-shift due to NBTI stress with and without plasma nitridation after gate etching and Fig. 13 shows Ion-Ioff characteristics for pMOS with and without plasma nitridation. By plasma nitridation treatment after gate etching, pMOS NBTI reliability is not degraded, and pMOS Ion-Ioff characteristic is improved.

5. Conclusion

We found that boron penetration from the S/D-extension becomes crucial issue on gate leakage, gate-oxide TDDB and NBTI characteristics, especially for deep sub-micron pMOS. We suggest that the plasma nitridation treatment after gate etching is the best solution for 65nm CMOS and beyond.

References

[1] K. P. Cheung *et al.*, VLSI Tech Dig. (1998), p. 198
[2] A. I. Chou *et al.*, Appl. Phys. Lett. **69** (7) (1996), p.934
[3] T. Yamashita *et al.*, to be presented in VLSI Sympo. 2004
[4] Y. Nakahara *et al,*. IEDM Tech. Dig. (2003), p.281

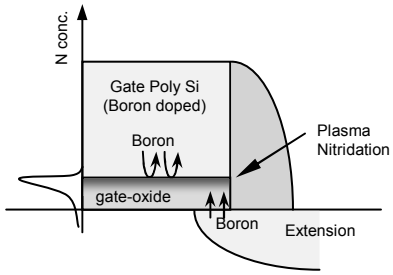

Fig. 1. Model for pMOS with SiON thin-film fabricated by plasma nitridation

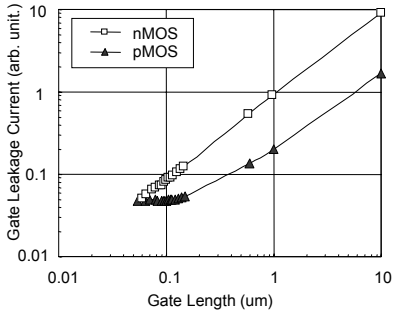

Fig. 2. Dependence of inversion gate leakage current on gate length.

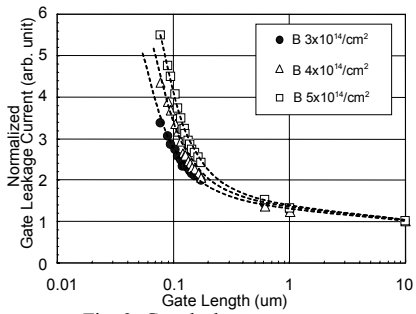

Fig. 3. Gate leakage current dependent on extension boron concentration

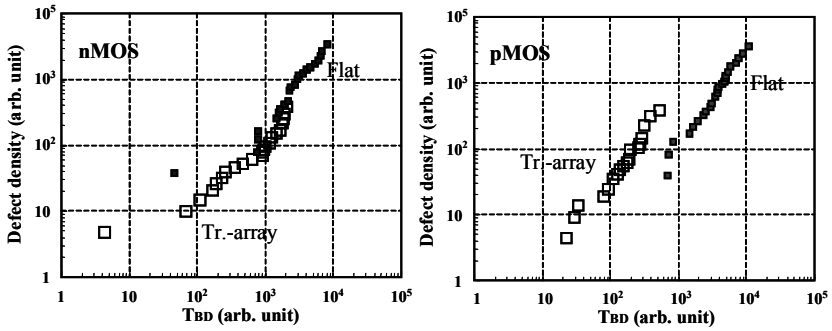

Fig. 4. Normalized T_{BD} distributions of flat capacitor and transistor array for nMOS and pMOS

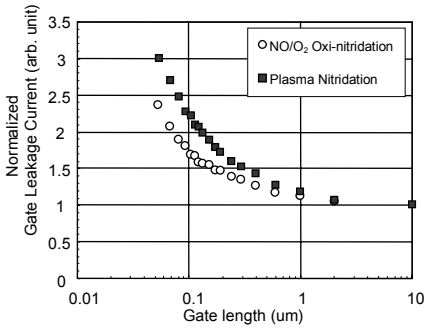

Fig. 5. Gate leakage current dependent on SiON fabrication process

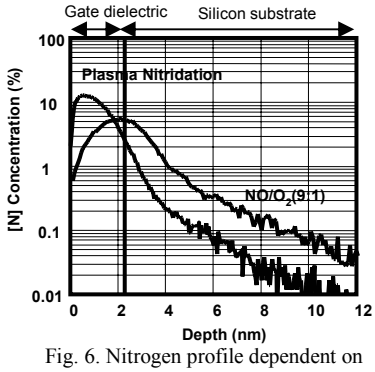

Fig. 6. Nitrogen profile dependent on SiON fabrication process

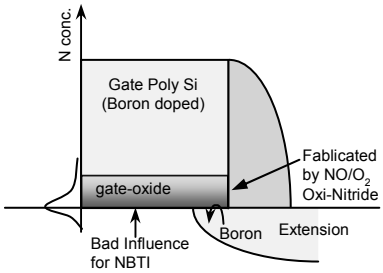

Fig. 7. Model for pMOS with SiON thin-film fabricated by NO/O_2 oxi-nitridation

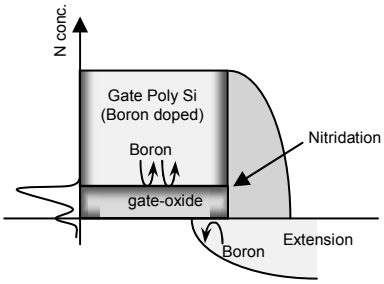

Fig. 8. Ideal nitrogen profile for pMOS

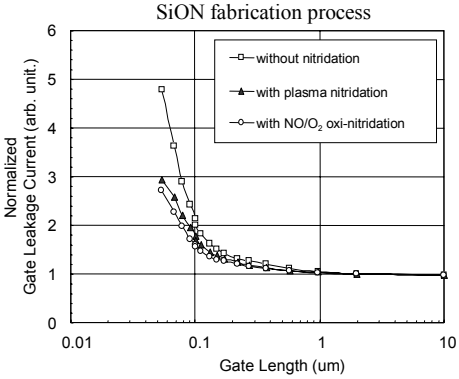

Fig. 9. Gate leakage current dependent on treatment after gate etching.

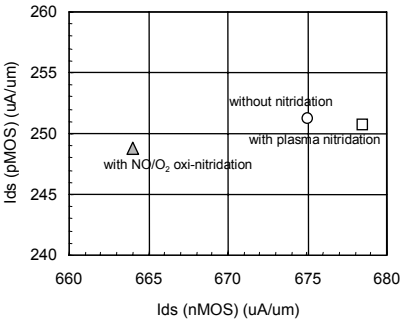

Fig. 10. Drive current dependent on treatment after gate etching

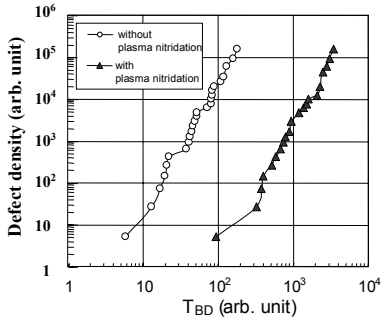

Fig. 11. Dependence of T_{BD} distribution of pMOS on treatment after gate-etching.

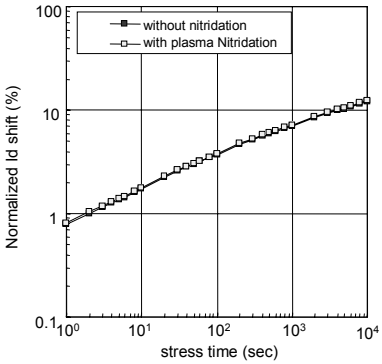

Fig. 12. Id-shift due to NBTI stress for pMOS with/without plasma nitridation after gate etching

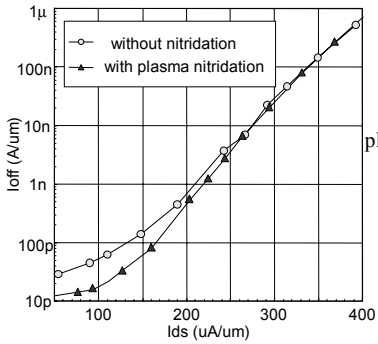

Fig. 13. Id-Ioff charactoristics for pMOS with/without plasm nitridation after gate etching