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Dopant Profile Design Methodology for 65 nm Generation via Inverse Modeling

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Abstract We have applied inverse modeling technique to analysis and design of scaling for 65 nm generation MOSFETs. Our model has well described trade-off relation between drive current and tolerance to short channel effect. Using the model, we have succeed to clarify specific problems of the present device and to quantitatively design a future targeted device.

1 Introduction In the scaling of advanced MOSFET, drive current $I_{\rm on}$ often decreases even though gate length $L_{\rm gate}$ shorten among the same $I_{\rm off}$ [1] due to short channel effect (SCE) and parasitic resistance at the gate edge. To suppress the SCE, FD SOI or double gate are candidates for high performance application. On the other hand, conventional MOSFETs is still main candidate for low operation power and low stand-by power application [2]. To scale conventional MOSFETs many approaches are possible: thinner $T_{\rm ox}$, larger mobility, steeper $X_{\rm j}$, high-k gate insulator and so on. However, they are always in a complex trade-off relation and it is difficult to expect those actual performance.

In this paper, we have applied inverse modeling (IM) technique to analyze and design for scaling of conventional MOSFETs. Our careful modeling has succeeded to well describe the complex trade-off relation in scaling. We present practical scheme to design new generation technology.

2 Reproduction of properties via inverse modeling Our methodology consists of tree steps (Fig. 1): (1) extract and reproduce the properties in the present device by modeling, (2) analyze the reason why the performance is limited, (3) evaluate and expect what and how large should be improved for the future targeted generation. We discuss them in the following.

First, we have prepared a sample set fabricated by 90 nm generation technology with different pocket dose condition to study relation between device performance and suppression of SCE. Measurement shows (1) a trade-off that shorter $L_{\rm min}$ (defined by $L_{\rm eff}$ at $I_{\rm off} = 1$ μA/μm) gives smaller $I_{\rm on}$, (2) much better $I_{\rm on}$ in indium pocket than in boron one (Figs.2, 3).

To model those properties, we have applied our IM method [3–5] and the generalized hydrodynamic model [6, 5]. The former has an advantage to analyze 2D profile effect and continuous change of the SCE [4], and the latter is well refined and proved to be valid for $L_{\rm eff} \sim 20$ nm [5]. Those two key technologies are important because drive current is affected by both 2D profile effect (i.e. DIBL) and non-equilibrium transport effect (i.e. velocity overshoot). To correctly reproduce the complex trade-off relation, the model well refined by us was required (Figs. 2, and 3).

3 Analysis of what limits scaling Second, we analyze what is the origin of (1) the trade-off relation and (2) pocket dopant dependence shown in Fig. 3.

The pocket dose amount dependence of $I_{\rm on}$–$L_{\rm min}$ properties is understood by several reasons as follows. Even though shorter gate length, g_m degrades because heavier pocket dose degrades the inversion layer mobility and the effect surpasses the merit of shorter channel length (Fig. 4(a)). In addition, electric field from drain decreases gate controllability in the shorter one. Moreover, the worse S-factor in the shorter MOSFETs results deeper threshold voltage in the linear scale ($V_{\rm th\,lin}$), which leads to worse $I_{\rm on}$(Fig. 4(b)).

Comparing boron pocket, indium pocket has smaller S-factor though it has retrograde channel profile. The reason is, in the indium pocket, electric field from the drain is well suppressed by pocket dopant and electric field much concentrates to the channel(Fig. 5). In addition, thinner dopant at the source edge results larger mobility.

This investigation has clarified that the performance of our samples is limited mainly by strong electric field from the drain. Thus, we conclude that the most effective breakthrough is in the improvement of the extension $X_{\rm j}$.

4 Design and approach to 65 nm generation MOSFETs Here, we discuss design of 65 nm generation MOSFETs for low operation power application at 2007.

$T_{\rm ox}$ scaling is often expected to improve not only drive current but also tolerance to SCE. However, our simulation (Figs. 6(a), 8) shows it improves only $I_{\rm on}$ in this case. In high-k gate insulator, $I_{\rm on}$ is smaller and $L_{\rm eff}$ is larger than that of SiON with the same EOT, because electric field from drain passes through the gate insulator and weakens gate controllability (Fig. 7). The mobility enhancement by strained-Si or stress from STI also enlarges $I_{\rm on}$ but $L_{\rm eff}$ remains large (Fig. 6(b)).

To operate at the scaled $L_{\rm min}$, steeper extension is most important (Fig. 8). It is consistent with the discussion at the previous section. Our calculation found a solution that steeper extension (horizontally half and vertically half) realizes the operation at $L_{\rm min} = 23$ nm and we will reach the target by some more improvement (such as channel profile engineering, $R_{\rm sd}$ reduction, mobility enhancement). We note that high-k gate insulator is never inevitable.

5 Conclusion Our modeling technique (inverse modeling and transport modeling) is effective to well describe complex trade-off relation between drive current and tolerance to short channel effect and clarify the specific problems in the present device. Our scheme with this technique is efficient to design MOSFETs scaling for the 65 nm generation and beyond.

References

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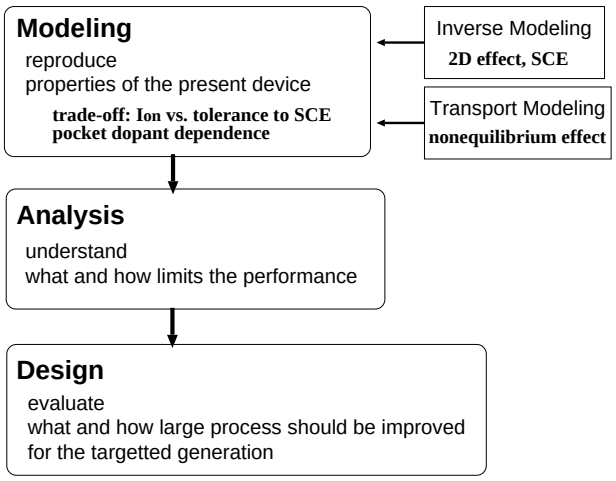

Figure 1: Scheme of process design for the future technology generation.

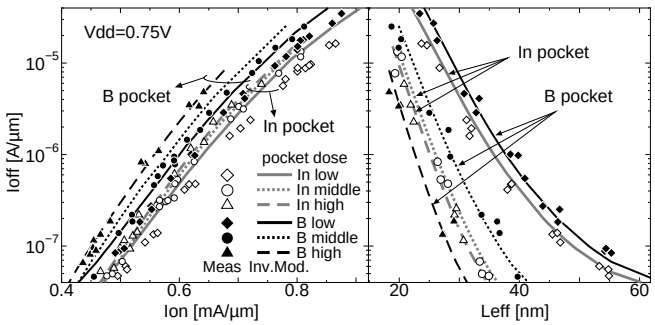

Figure 2: $I_{\rm on}$–$I_{\rm off}$ and $L_{\rm eff}$–$I_{\rm off}$ comparing measurement and calculation by inverse modeling for all samples.

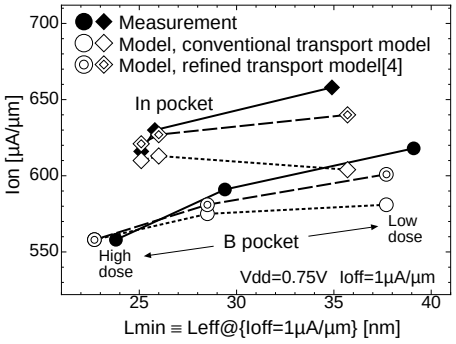

Figure 3: Trade-off relation of $I_{\rm on}$ vs. $L_{\rm min}$ among different pocket dose amount and dopant. $L_{\rm min}$ is defined by the effective gate length $L_{\rm eff}$ which gives $I_{\rm off} = 1$ μA/μm at $V_d = 0.75$ V.

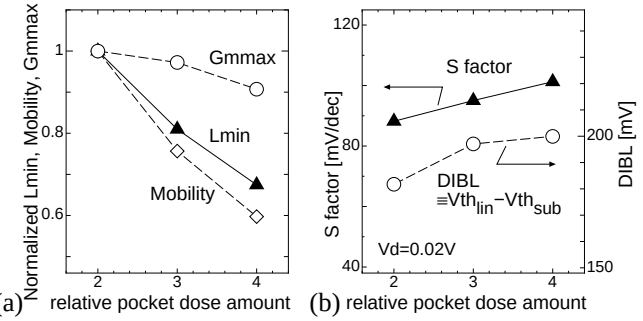

Figure 4: Pocket dose amount dependence of (a) normalized $L_{\rm min}$, electron mobility at source edge, $g_{m\,\max}$, and (b) S factor and DIBL defined by difference between $V_{\rm th}$ at linear scale and $V_{\rm th}$ at constant subthreshold current.

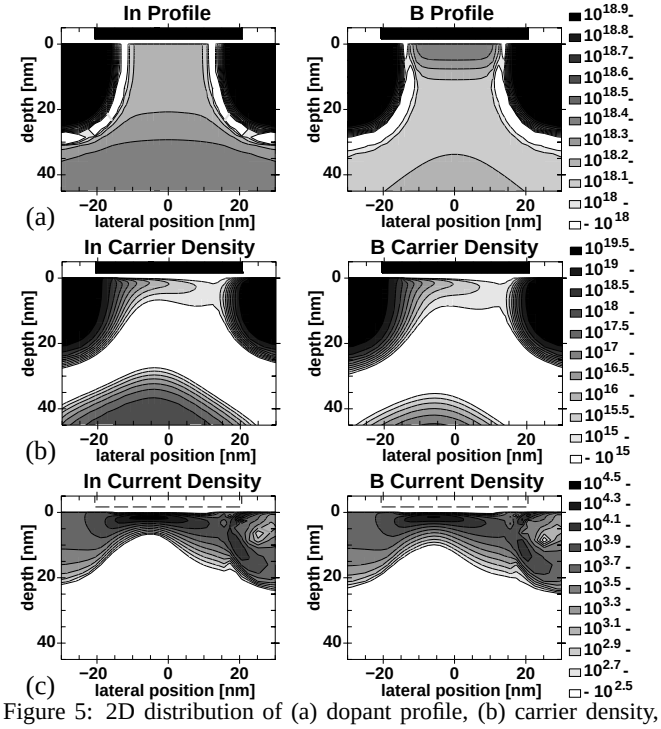

Figure 5: 2D distribution of (a) dopant profile, (b) carrier density, and (c) current density in MOSFETs with (left) indium and (right) boron pocket. The MOSFETs have the same $I_{\rm off} = 1$ μA/μm and $L_{\rm eff} = 25.1$ nm at $V_{dd} = 0.75$ V. The carrier density and the current density is calculated at $V_g = 0$ V, $V_d = 0.75$ V.

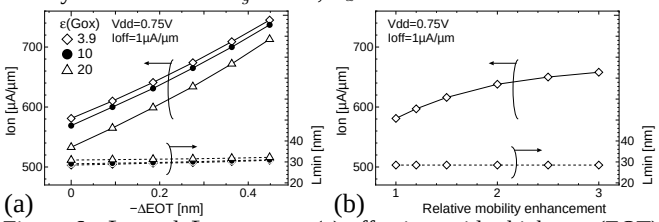

Figure 6: $I_{\rm on}$ and $L_{\rm min}$ versus (a) effective oxide thickness (EOT) reduction and (b) relative enhancement of low field inversion layer mobility.

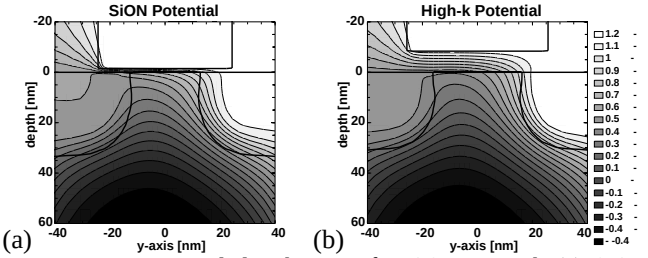

Figure 7: 2D potential distribution of MOSFETs with (a) SiON (ϵ=3.9) and (b) high-k (ϵ=20) gate insulator at $V_g = V_d = 0.75$ V. The MOSFETs have the same $I_{\rm off} = 1$ μA/μm at $V_{dd} = 0.75$ V.

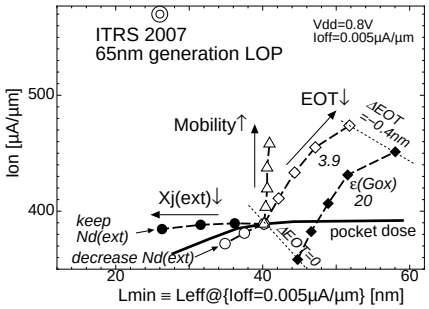

Figure 8: Process sensitivity to $I_{\rm on}$–$L_{\rm min}$ on (a) decrease of EOT [ϵ(Gox) =3.9, 20], (b) increase of inversion layer mobility, and (c) decrease of $X_{\rm j}$ of extension [with and without decrease of extension peak density N_D(ext)]. The ITRS roadmap [2] target for low operation power in 65 nm generation at 2007.