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Strained-Si for CMOS 65nm node : $Si_{0.8}Ge_{0.2}$ SRB or "Low Cost" approach ?

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1. Introduction

Recently, many strained-Silicon (s-Si) approaches have been demonstrated in order to enhance the device performance [1-5]. The power supply reduction as well as the increase of the transistor access resistance made this solution mandatory for 65nm node and below. While pMOS device are intrinsically strained by the layout scaling [6,7], nMOS is strongly degraded. In this work, two different s-Si approaches for nMOS enchancement are compared. The first one consists in using $Si_{0.8}Ge_{0.2}$ substrate relaxed buffer (SRB), to induce bi-axial tensile stress in Si channel inversion layer. The second approach, cheaper, consists into increasing the contact etch stop layer thickness in order to induce stress in Si-channel, and using a Ge implantation to avoid pMOS degradation.

2. S-Si MOSFETs on $Si_{0.8}Ge_{0.2}$ SRBs

SRBs consist in a step graded buffer, followed by a $Si_{0.8}Ge_{0.2}$ epitaxy (Fig 1a). After a specific STI formation, a 150Å Si epitaxy is made. This define the strained- Si channel of s-Si MOSFETs. After gate oxide formation (1.2nm EOT), and poly-Si gate deposition, gate is patterned down to 42nm (Fig 1b). Spacer formation is performed keeping a low thermal budget. Final activation anneal is made using fast spike annealing. Finally, salicidation is performed using Nickel. Gate oxide quality is not degraded by s-Si as shown on Fig 2a. Variation of SD resistance can be seen Fig 2b, is due to the enhanced As diffusion and reduced B diffusion. NiSi formation results into an increase of 23% of resistance (Fig 2c). This shows that a specific optimisation step in necessary when using the SRB approach. Finally, junction leakage is dramatically increased by over 2 decades (Fig 2d). Threshold voltage roll-off for nMOS is strongly impacted by the modification of As diffusion, and a specific optimisation step is mandatory. nMOS device saturation current improvement as a function of gate length Lg is plotted on Fig 3-4. At same overdrive (Fig 3), the measured gain is 15%-20% for L=55nm . At same Vth (Fig 4), if on long channel devices the gain is found to be close to 100%, it diminishes with Lg. This degradation of the improvement with Lg is fundamentally limited by device physics as predicted by MASTAR [9]. Moreover, because of the difference of conductivity between SiGe layer and Si layer, a self heating effect appears. This still reduces the saturation current by 5-10%.

3. Low Cost Strain-Si approach

A cheaper approach to obtain s-Si is to increase the thickness (T0) and the intrinsic stress of the so-called contact etch stop layer (CESL) [10-11]. A similar process flow as described in part 2 is applied for device fabrication. We increased the tensile CESL thickness up to 3 times its initial value, and performed an optional Ge implantation in order to locally relax the intrinsic stress [8], and subsequently reduce the pMOS performance degradation. At the contrary of the SRBs, this approach requires no further optimisation steps. The nMOS I_{Dsat} improvement as a function of gate length is shown on Fig.7. As L_g is reducing, the performance improvement is increasing, but saturates for sub-0.1µm devices. Nevertheless, this makes this technique extendable to the next technological nodes featuring even smaller gate lengths. In the present experiment, for Lg=45nm device up to 15.6% improvement is observed (Fig 8), leading to a device performance of I_{Dsat}=789µA/µm with I_{off}=88nA/µm for V_{dd}=0.9V, and I_{Dsat} = 920µA/µm with I_{off}=100nA/µm for V_{dd}=1.0V (Fig. 9). On pMOS device, Ge implantation limits the performance degradation (Fig 10). Fig.11 represents the I_{Dsat} improvement, as a function of the induced strain for both pMOS and nMOS On pMOS, degradation is kept close to -2%, while a saturation of the improvement effect on nMOS seems to appear for the higher strain values

4. Conclusion

Comparable improvement is obtained using SRB or CESL.

	SRB	CESL
Stress-type	Substrate	Process Induced
Integration	Specific	-
Max. efficiency	Long device	Short device
N IDsat Improvement Nominal device	15% *	15%
P IDsat Improvement Nominal device	-	-2%

* includes self-heating effect

Nevertheless, SRB approach requires a specific substrate, and integration scheme for STI, Junction and silicide process, making this integration a "high-cost" option. Nevertheless, for high performance application, the combination of SRB and CESL can be an interesting solution.

Acknowledgements

Reference:
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[7] V. Chan et al, IEDM 2003
[8] S. Ito et. al, IEDM 2000, pg. 247-251
[9] Model for Assesment of CMOS Technology

and Advanced Roadmaps (see http://public.itrs.net)
T.Skotnicki and F.Boeuf, ECS 2002
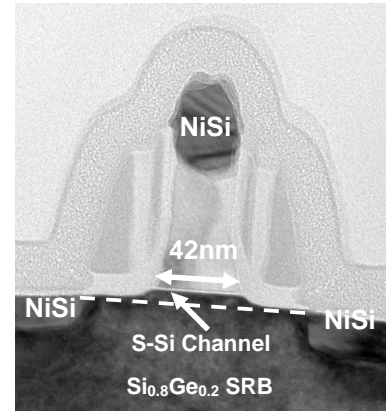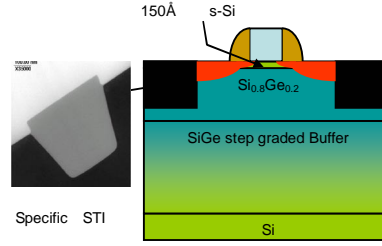[10] S. Thompson et al., IEDM 2002
[11] C. Diaz et al., IEDM 2003

Figure 1: (a) Schematic representation of the SRB integration, featuring a specific STI module (b)TEM cross-section of nominal device fabricated on $Si_{0.8}Ge_{0.2}$ SRB.
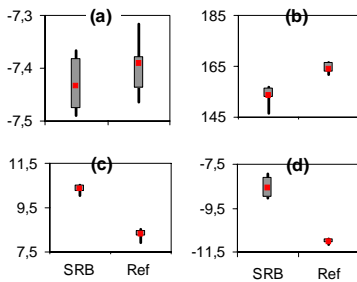
Figure 2: comparison of (a) gate leakage (b) SD resitance (c) Silicide Resitance and (d) Diode leakage
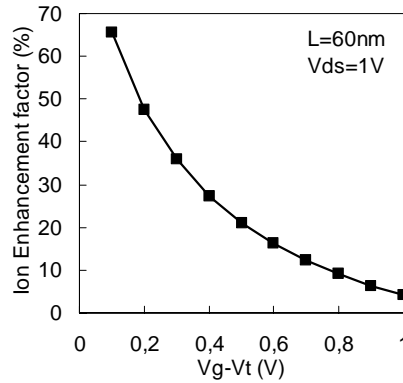
Figure 3 : IDsat enhancement as a function of gate overdrive. Despite self-heating impact, a 15% enhancement is observed for a 0.6V overdrive

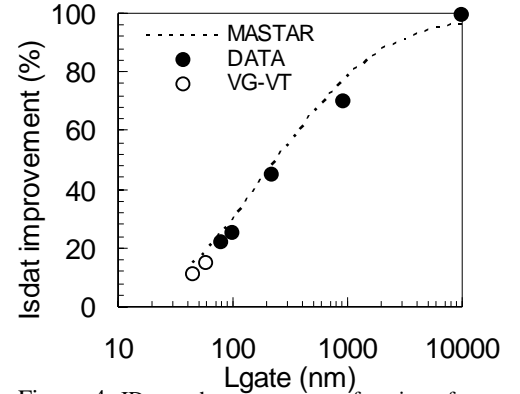Figure 4: IDsat enhancement as a function of gate length, at same Vth (black circle), and same over-drive (empy circle). Dotted line : MASTAR model
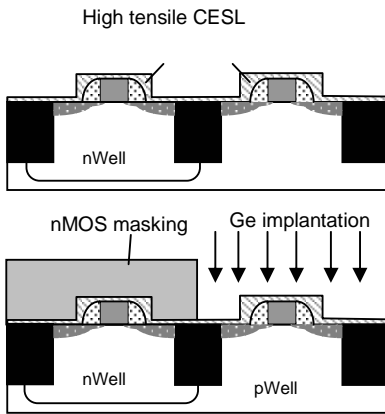

Figure 5 : low cost strained-Si integration scheme

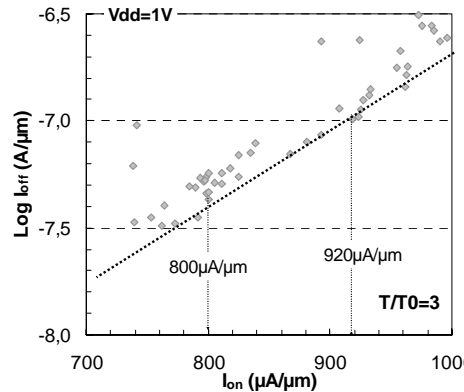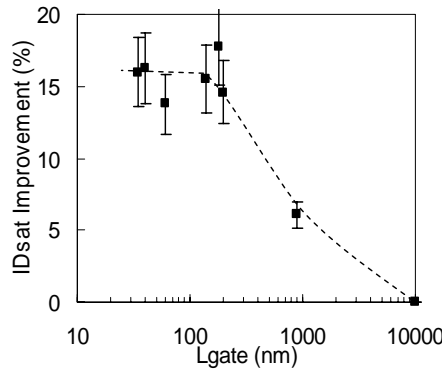Figure 7 : nMOS saturation current improvement as a function of gate length
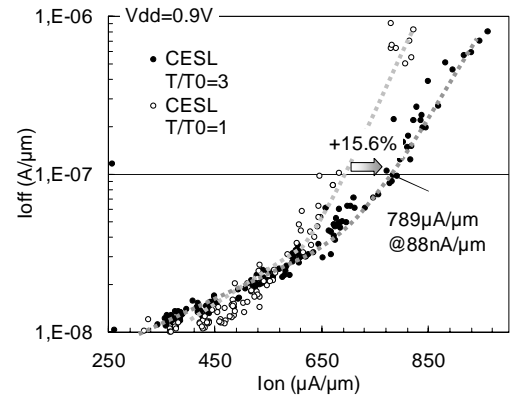
Figure 8: Ion/Ioff trade-off at Vdd=0.9V for un-strained and strained nMOS devices
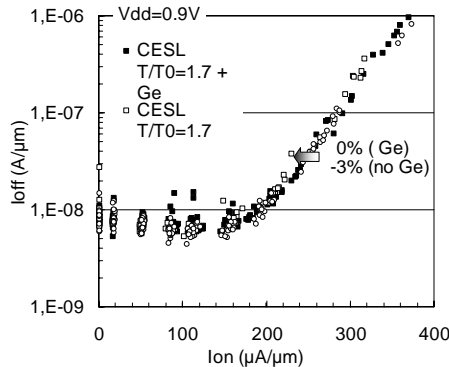

Figure 9: Ion/Ioff trade-off for strained nMOS devices at

Figure 10 : Impact of Ge implant on Ion/Ioff trade-off for pMOS devices for t/t0 = 1.7.
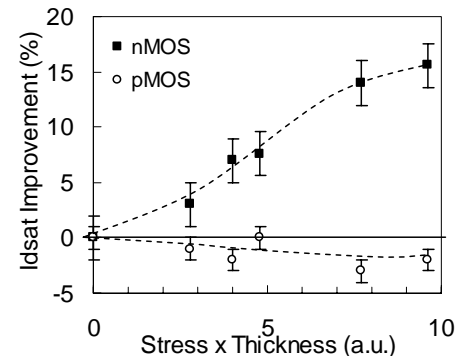

Figure 11 : I_{Dsat} variation as a function of applied strain for nMOS and pMOS devices