Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 738-739

A-10-3

A Quantum Mechanical Corrected SPICE Model for Ultrathin Oxide MOSFETs' Gate Tunneling Current Simulation

Yiming Li[1,2,*] Shao-Ming Yu[3], and Jam-Wem Lee[1]

[1]Department of Computational Nanoelectronics, National Nano Device Laboratories
[2]Microelectronics and Information Systems Research Center, National Chiao Tung University
[3]Department of Computer and Information Science, National Chiao Tung University
*Corresponding author. Address: P.O. BOX 25-178, Hsinchu City, Hsinchu 300, TAIWAN; E-mail: ymli@mail.nctu.edu.tw

1. Introduction

Accurate gate tunneling current model plays an important role for nanoscale device modeling and gigascale circuit simulation, in particular for the modern ultrathin oxide MOSFETs and SOC era [1-19]. For sub-100 nm CMOS devices, the gate oxide thickness can be as thin as 1 nm. For such ultrathin gate oxides, a substantial direct tunneling current flowing from the gate to the channel results in a gate leakage current even under low voltage operating condition; furthermore, I_g increases exponentially when T_{ox} decreases. The significant leakage current becomes a serious problem, especially in terms of the standby power consumption. For physical modeling of nanoscale devices, various QM approaches have been of great interest [8-14]. However, they may not suit for compact models and VLSI circuit simulation. Various gate current formulas (analytical and semi-analytical models) have been proposed for I_g calculation and have their merits [1-19]. It is found that the gate leakage current calculated with classical (CL) potential is always underestimated and the circuit performance becomes greatly overestimated. To precisely and efficiently perform the calculation of I_g in circuit simulation, incorporating the QM effects into SPICE models in a full analytical way is necessary, especially designing the nanoscale MOSFETs' VLSI circuits.

In this paper, a full analytical quantum correction model for gate tunneling current (I_g) calculation of ultrathin oxide MOSFET devices is proposed. In the model formulation, the quantum mechanical (QM) surface potential in the channel region is considered analytically. Compared with the conventional approach to I_g calculation, the proposed model shows very good agreement with TCAD simulation. Consequently, the physically meaningful results are achieved. Comparison of the results with the measured I_g of MOSFET with different untrathin gate oxides (T_{ox} = 1.0, 1.2, and 1.5 nm) practically confirms the validity of the model. Mathematically, this quantum-corrected analytical model is explicit and continuous with respect to variables. It can directly be implemented into SPICE tool for advanced VLSI circuit simulation.

2. A SPICE-Compatible Gate Tunneling Model

By following the Tsu–Esaki tunneling current formula [15-19], the gate tunneling current, shown in Fig. 1, is known as $J_g = J_0 \int D(E)F_s(E)dE$, where J_0, D(E) and $F_s(E)$ are the transmission coefficient and the supply function at the given kinetic energy E. In general, the integral in the formula above is calculated numerically and prohibits it to be incorporated into SPICE models for circuit simulation. The most of electrons occupy the states close to the band edge. Therefore, we may assume here that all the tunneling takes place at a constant energy, E_T, and $J_g = J_0 D(E_T)F_s(E_T)$, where $F_s = \ln((1 + \Delta_{si}) / (1 + \Delta_{poly}))$, $\Delta_{si} = \exp((E_f^{si} - E_T) / k_BT)$, and $\Delta_{poly} = \exp((E_f^{poly} - E_T) / k_BT)$. E_f^{si} is the Fermi level of silicon substrate and E_f^{poly} is the Fermi level of the polysilicon gate. At equilibrium condition, $F_s = 0$ and $J_g = 0$. WKB approximation gives $D(E_T) = \exp(B(G_1 + G_2(|V_{ox}| / X_B)(1 + G_3(|V_{ox}| / X_B))))$, where $B = (2T_{ox} / \hbar)(2qm^* X_{BT})^{1/2}$, $X_{BT} = X_B - E_T$, and $E_T = E_{cs}^{si} + 0.5(((V_{ox} - G_0V_T)^2 + 10^{-3})^{1/2} - (V_{ox} - G_0V_T))$. E_{cs}^{si} is the surface potential energy, V_T = 0.0259 eV, and V_{ox} is a drop across the gate oxide. The CL surface potential is now explicitly written as $0.03 + 0.026\ln(N_A) - 0.026T_{ox} + 0.1V_g - 0.01\,T_{ox}V_g$, and QM surface potential is given by $0.08 + 0.026\ln(N_A) - 0.036\,T_{ox} + 0.2V_g - 0.02\,T_{ox}V_g$, where T_{ox} is in nm, V_g is in Volt, N_A is with cm^{-3}. The model validity is tested with N_A varying from 10^{16} cm^{-3} to 10^{18} cm^{-3}. The equations above form a completely analytical I_g model for circuit simulation. G_0-G_3 are the model parameters to be calibrated and optimized with the results of QM model [11-14].

3. Results and Discussion

As shown in Fig. 2, the optimized G_0-G_3 are device structure- and bias-dependent. The difference of G's value is significant when the CL and QM surface potentials are used in the calculation of I_g. The difference increases when T_{ox} decreases. Compared with the QM TCAD simulation [8-14], shown in Fig. 3, the I_g model together with the QM surface potential formula shows better accuracy than that of CL potential. In addition, I_g is measured and compared with the fabricated N-MOSFETs with 3 ultrathin T_{ox}. As shown in Figs. 4, 5, and 6, the agreements between the measured and simulated I_g are excellent for the N-MOSFET with T_{ox} = 1.0, 1.2, and 1.5 nm, respectively. The figures also show that the quantum correction on the surface potential plays an important role in accurate calculation of I_g. Using the same model, the difference of the calculated I_g with and without quantum correction on the surface potential is up to 1-2 orders magnitude. It increases when T_{ox} decreases.

4. Conclusions

In conclusion, we have presented a full analytical quantum correction model for gate tunneling current calculation in ultrathin oxide MOSFET devices. Comparison of the results with the measured I_g of MOSFET with different T_{ox} confirmed the model validity. It works well for ultrathin oxide MOSFETs and can be implemented into SPICE tool for VLSI circuit simulation.

Acknowledgements

This work is supported in part by the National Science Council (NSC) of TAIWAN under contract No.: NSC – 92 – 2112 – M – 429 – 001 and the grant of the Ministry of Economic Affairs, Taiwan under contract No. 92 – EC – 17 – A – 07 - S1 – 0011.

References

[1] A. J. Scholten *et al*., Tech. Dig. IEDM (2002) 129.

[2] M. M. A. Hakim *et al*., IEEE T ED **49** (2002) 1669.
[3] L. Mao *et al*., *Microelec. Reli.* **42** (2002) 175.
[4] A. Ghetti, Microelec. Eng. **59** (2001) 127.
[5] L. Mao *et al*., Solid-State Elec. **45** (2001) 53.
[6] N. Yang *et al*., Microelec. Reli. **41** (2001) 37.
[7] C.C. McAndrew *et al*., IEEE T ED **49** (2002) 72.
[8] W.-C. Lee and C. Hu, Proc. VLSI Symp. (2000) 203.
[9] S.-H. Lo *et al*., IEEE EDL **18** (1997) 209.
[10] Y.-K. Choi *et al*., Jpn. JAP **42** (2003) 2073.

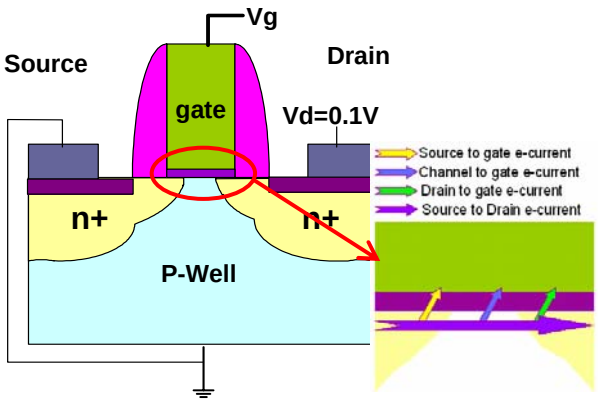

Fig. 1 The measurement of the gate tunneling current.

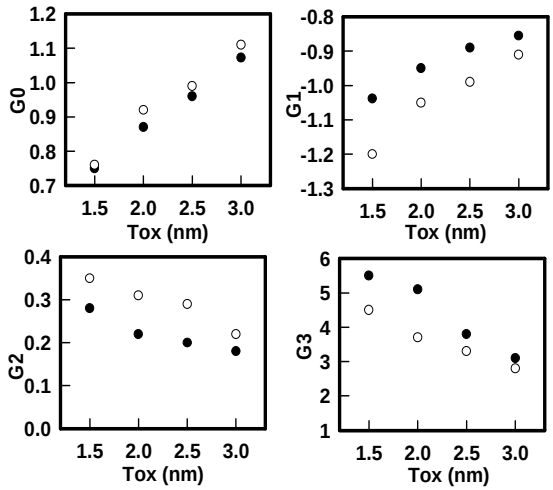

Fig. 2 The optimized G_0-G_3 with a Schrödinger-Poisson Solver [11-13]. The filled-in dots are the model with QM surface potential and the open dots are the model with CL surface potential.

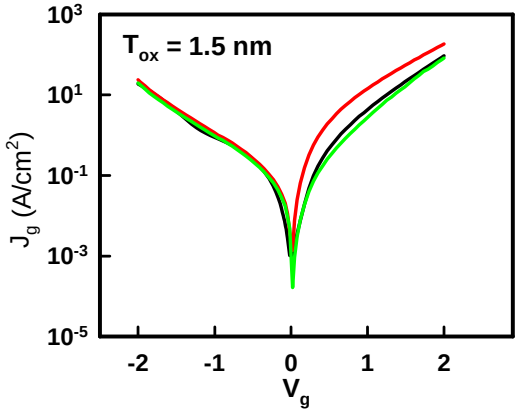

Fig. 3 Gate tunneling current comparison. The model using the CL (red line) and QM (green line) surface potentials. The black line is the QM simulation using our own Schrödinger-Poisson solver [11-13].

[11] Y. Li *et al*., IEEE T Nanotech. **1** (2002) 238.
[12] T.-w. Tang and Y. Li, IEEE T Nanotech. **1** (2002) 243.
[13] Y. Li *et al*., Comput. Phys. Commun. **147** (2002) 214.
[14] Y. Li and Y.Y. Cho, Jpn. JAP **43** (2004) 1717.
[15] R. Tsu and L. Esaki, APL **22** (1973) 562.
[16] K. M. S. V. Bandara and D. D. Coon, JAP **66** (1999) 693.
[17] A. Gehring *et al*., Elec. Lett. **39** (2003) 691.
[18] X. Gu *et al*., IEEE T ED **51** (2004) 127.
[19] M. Zervosa, JAP **94** (2003) 1776.

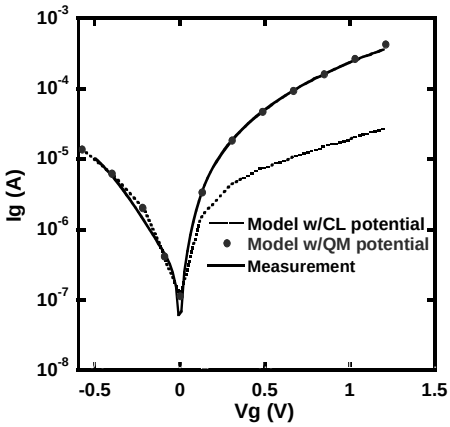

Fig. 4 The calculated I_g using the model with the CL and QM surface potentials, respectively. The solid line is the measured data. The N-MOSFET sample is with T_{ox} = 1.0 nm. We found that the I_g difference is up to 2-order magnitudes when V_g = 1.2 V.

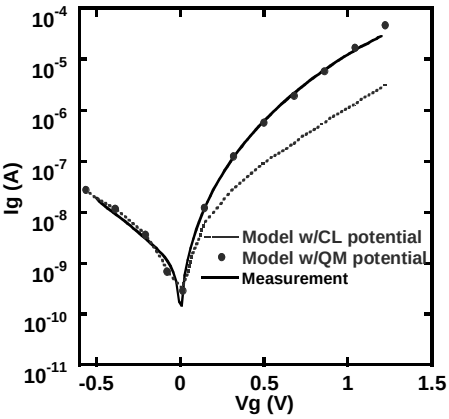

Fig. 5 The calculated I_g using the model with the CL and QM surface potentials. The solid line is the measured data, where the sample is with T_{ox} = 1.2 nm.

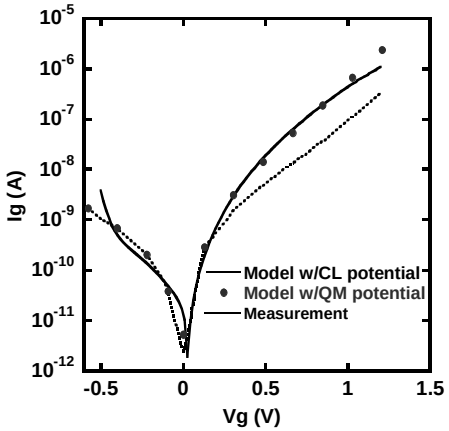

Fig. 6 The calculated I_g using the model with the CL and QM surface potentials, where the sample is with T_{ox} = 1.5 nm. Figs. 4-6 suggest that the QM surface potential significantly determines the accuracy of analytical I_g models.