

Fully Silicided NiSi Gates on HfSiON Gate Dielectrics for Low Power Application

Kenzo Manabe, Kensuke Takahashi, Taeko Ikarashi, Ayuka Morioka, Heiji Watanabe, Takuya Yoshihara, and Toru Tatsumi

System Devices Research Laboratories, NEC Corporation
1120, Shimokuzawa, Sagami-hara, Kanagawa 229-1198, Japan
Phone: +81-42-771-2294, Fax: +81-42-771-2481, E-mail: k-manabe@ce.jp.nec.com

1. Introduction

For future low power CMOS devices, several-orders-of-magnitude reduction in gate leakage current (I_g) is required compared to the poly-Si/SiO₂ devices at an equivalent oxide thickness (EOT) less than 2 nm. For instance, in 65nm node, I_g should be as low as 10^{-3} A/cm² at an EOT of 1.6 nm (i.e. capacitance equivalent thickness (CET) in inversion (T_{INV}) of 2.4 nm) [1]. For that purpose, high-k gate dielectrics have been studied extensively. HfSiON is a promising candidate for a high-k gate dielectric because of its excellent electrical properties [2,3]. However, when using poly-Si gate electrode, the Fermi level (E_F) pinning at the poly-Si/HfSiON interface causes both threshold voltage (V_{th}) shift and a large gate depletion in PMOS [4]. Thus, we consider that the combination of metal gate and HfSiON should be a possible way to overcome these problems.

Fully silicided (FUSI) metal gates have received increasing attention due to the simple integration scheme [5]. NiSi has a midgap work function on SiO₂, which makes it a promising metal gate candidate for low power CMOS application [6]. However, there have been few reports which investigate the impact of the combination of FUSI-NiSi gate and high-k gate on device performance except FUSI-NiSi/La₂O₃ MOSFET reported by Lin et al [7].

In this paper, for the first time, we demonstrate that FUSI-NiSi/HfSiON MOSFET can exhibit excellent transistor performance. We find that NiSi on HfSiON also has a midgap work function (4.5-4.55 eV), which reduces V_{th} shift of PMOS by 0.15 V. At the same time, I_g of 10^{-3} A/cm² at $T_{INV} = 2.1$ nm is achieved due to the elimination of gate depletion. Moreover, we can obtain the excellent carrier mobility for the NiSi/HfSiON transistors (PMOS:100%, NMOS:90%). These results show that NiSi/HfSiON gate stack is a promising candidate for low power CMOS applications in 65nm node.

2. Experimental

We fabricated NMOS and PMOS FETs using a replacement gate technique. The process flow is shown in Fig. 1. We prepared HfSiON films and the reference SiO₂ as gate dielectrics. After poly-Si gate formation, an activation anneal was performed at 950°C for 10 sec. The silicide gates were formed by annealing 140 nm Ni films on poly-Si at 400-600°C for 1 min. NMOS and PMOS devices with poly-Si gates were also fabricated for comparison.

3. Results and Discussion

Figure 2 shows C-V characteristics of PMOSFETs. For poly-Si/HfSiON, a large gate depletion is evident with T_{INV} (3.2 nm) being thicker by 1.1 nm than the CET in accumulation ($T_{ACC} = 2.1$ nm). This depletion is much larger than a normal poly-Si gate depletion (0.5-0.6 nm) and is

caused by an additional anomalous depletion (0.5-0.6 nm) due to the Fermi level pinning at poly-Si/HfSiON interface [4]. On the other hand, both T_{INV} and T_{ACC} for NiSi/HfSiON are 2.1 nm. This result shows that silicidation proceeded to the electrode/dielectric interface, and thus, gate depletion is eliminated. From the flatband voltage, the effective work function of NiSi on HfSiON is estimated to be 4.5-4.55 eV, which is close to Si midgap (4.6 eV), but the E_F is located at 0.05-0.1 eV above midgap.

Figure 3 is the difference in V_{th} from that for the poly-Si/SiO₂ devices (V_{th} shift). The use of NiSi gate can suppress the V_{th} shift for PMOS by 0.15 V compared to the poly-Si/HfSiON MOSFETs, whereas it increases the V_{th} shift for NMOS by 0.15 V. Such a change of V_{th} shift is explained by the difference between the E_F pinning level at poly-Si/HfSiON interface and the E_F of NiSi as illustrated in Fig. 4. The V_{th} shifts of poly-Si/HfSiON for PMOS (-0.75 V) and NMOS (0.25 V) in Fig. 3 indicate that the E_F pinning level is located at 0.7-0.8 eV above the top of valence band of Si (E_v). Therefore, by replacing poly-Si by NiSi, the E_F of PMOS gate approaches E_v , which causes the reduction of 0.15 V in V_{th} shift.

Figure 5 shows relationship between I_g and T_{INV} of PMOSFETs. For poly-Si/HfSiON, the magnitude of I_g reduction at the same T_{INV} is nearly one decade compared to the poly-Si/SiO₂ device. By replacing poly-Si by NiSi, we can reduce T_{INV} from 3.2 nm to 2.1 nm due to the elimination of gate depletion. Since I_g increase due to the T_{INV} reduction is not significant (factor of three), we achieved $I_g = 10^{-3}$ A/cm² at $T_{INV} = 2.1$ nm (five orders of magnitude reduction in I_g compared to the poly-Si/SiO₂).

The Id-Vg characteristics are shown in Fig. 6. All the devices show good sub-threshold characteristics, which indicate that full silicidation does not degrade the electrical properties at the HfSiON/Si interfaces.

Figure 7 shows the mobility of NiSi/HfSiON and the reference poly-Si/SiO₂ MOSFETs. NiSi/HfSiON PMOS device does not show the mobility degradation (100% of the reference transistor). The mobility of NiSi/HfSiON NMOS at 0.8-1 MV/cm is 80-90% of that of the reference MOSFET. These carrier mobilities are much higher than those of FUSI-NiSi/La₂O₃ devices (50-60% of that of poly-Si/SiO₂ device) [7]. We speculate that the reported mobility degradation was caused by a high interfacial trap density and/or metal diffusion into gate dielectric during annealing. The obtained high carrier mobility for our devices may come from the excellent electrical properties at the HfSiON/Si interfaces [3] and the suppression of Ni diffusion, which are suggested by the good sub-threshold characteristics.

Figure 8 is the comparison of Id for the poly-Si/HfSiON and NiSi/HfSiON PMOSFETs. For the NiSi/HfSiON device, 85% increase in Id is achieved compared to the poly-Si/HfSiON MOSFETs. This can be

explained by three factors; the elimination of gate depletion(45% Id increase), the suppression of V_{th} shift(55% Id increase) and a slight mobility decrease due to higher effective field, E_{eff} (15% Id decrease, see Fig. 7), which is caused by reduction in T_{INV} .

4. Conclusion

For the first time, we demonstrate that FUSI-NiSi/HfSiON MOSFET can exhibit excellent transistor performance. We find that midgap work function for NiSi on HfSiON(4.5-4.55 eV) reduces V_{th} shift of PMOS by 0.15 V. I_g of 10^{-3} A/cm² at $T_{INV} = 2.1$ nm is achieved due to the elimination of gate depletion. We can also obtain the excellent carrier mobility for the NiSi/HfSiON transistors(PMOS:100%, NMOS:90%). These results show that NiSi/HfSiON gate stack is a promising candidate for low power CMOS applications in 65nm node.

Acknowledgements

The authors would like to thank Dr. Nobuyuki Ikarashi for his useful discussions. The authors also would like to express their appreciation to Dr. Yasunori Mochizuki and Dr. Masao Fukuma for their encouragement during this work.

References

- [1] ITRS Roadmap 2003.
- [2] A. L. P. Rotondaro et al., Symp. VLSI Tech., (2002) 148.
- [3] T. Iwamoto et al., IEDM Tech. Dig., (2003) 639.
- [4] C. Hobs et al., Symp. VLSI Tech., (2003) 9.
- [5] B. Tavel et al., IEDM Tech. Dig., (2001) 825.
- [6] J. Kedzierski., IEDM Tech. Dig. (2003) 315.
- [7] C. Y. Lin et al., IEEE Electron Dev. Lett., vol.24, (2003) 348.

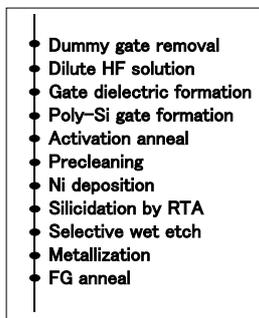


Fig. 1 Fabrication process flow.

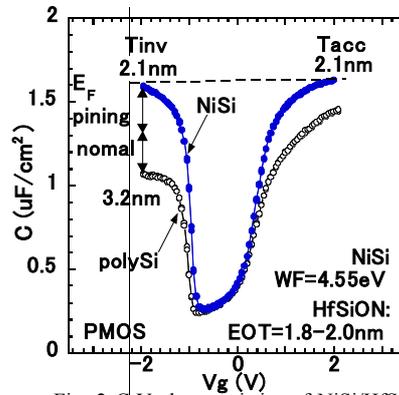


Fig. 2 C-V characteristics of NiSi/HfSiON and poly-Si/HfSiON PMOSFETs.

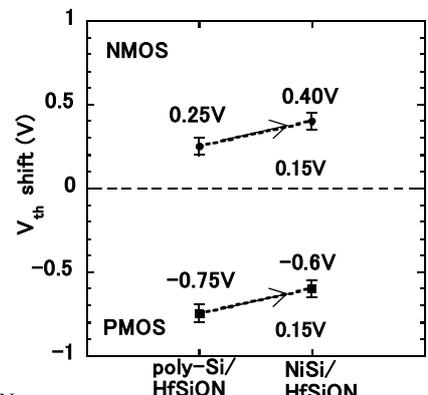


Fig. 3 V_{th} shifts compared to the poly-Si/SiO₂ devices.

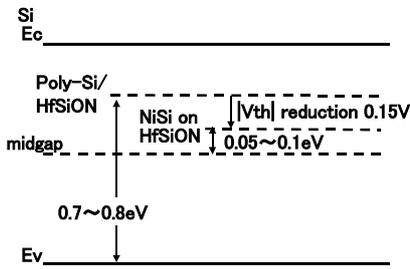


Fig. 4 Relationship between the pinning level at the poly-Si/HfSiON interface and the Fermi level(E_F) of NiSi on HfSiON.

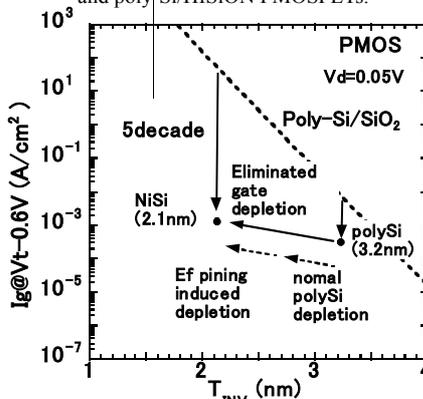


Fig. 5 I_g - T_{INV} relationship of NiSi/HfSiON and poly-Si/HfSiON PMOSFETs.

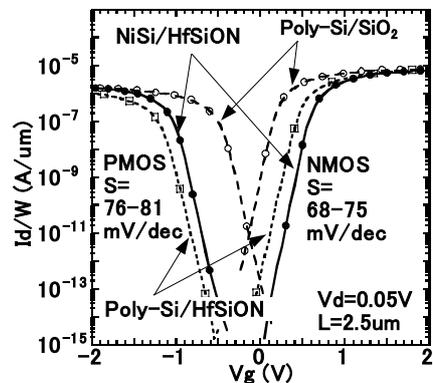


Fig. 6 I_d - V_g characteristics.

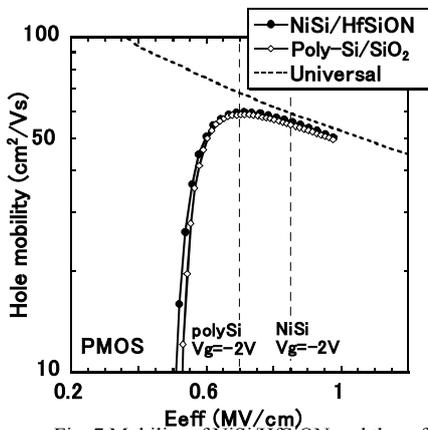


Fig. 7 Mobility of NiSi/HfSiON and the reference poly-Si/SiO₂ MOSFETs. Vertical dashed lines indicate E_{eff} for poly-Si/HfSiON and NiSi/HfSiON gate stack when $V_g = -2$ V.

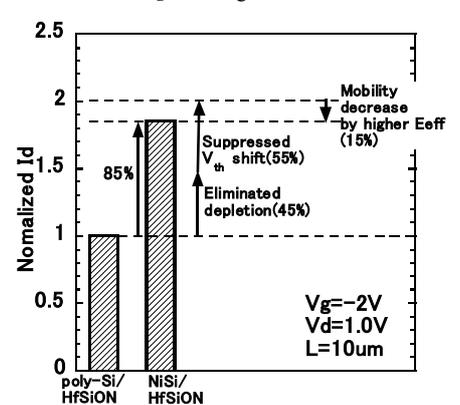
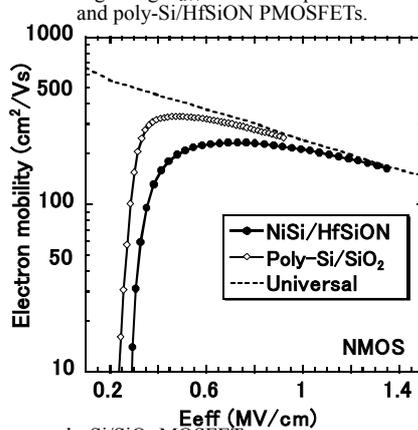


Fig. 8 Comparison of I_d of the poly-Si/HfSiON and NiSi/HfSiON PMOSFETs.