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High Mobility Dual Metal Gate MOS Transistors with High-k Gate Dielectrics

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1. Introduction

In 45nm technology node and beyond, metal gate(MG) electrodes are required to eliminate gate depletion problems that are associated with conventional poly-Si gates. Recently, poly-Si gates have been shown to suffer also from Fermi level pinning on high-k gate dielectrics.[1]

So far, several types of MG/High-k material systems have been studied: Ta, TaN, and TaSiN have been suggested as promising materials for NMOS, while TiN suggested for PMOS, when combined with the high-k dielectric materials such as HfO_2, Al_2O_3.[2,3] Unfortunately carrier mobilities in these previous studies were reported to be very low as compared with that for poly-Si/SiO_2 stack possibly due to a large number of residual charges in the high-k gate dielectrics and/or due to a sensitivity to process damage.[4] From such a viewpoint, HfSiO is worth studying since it offers excellent device performance when stacked with poly-Si gate.[5] But, its metal gate study has been scarcely reported.

In this study, by utilizing the established high quality of HfSiO and also by minimizing the processes damage during the MG formation process, we demonstrate high carrier mobility and low leakage currents ($1x10^{-3}A/cm^{-2}$) for inversion equivalent oxide thickness (Tinv) down to 1.7nm. Furthermore, workfunctions (WF) for metals on HfSiO are characterized and it is found that Ta/HfSiO-NMOS and TiN/HfSiO-PMOS transistors yield symmetrical threshold voltages (Vth). These results suggest that HfSiO is promising for MG/high-k gate transistors.

2. Experimental

The MG/high-k MOS transistors were fabricated by using replacement gate process as shown in Fig. 1. We used HfSiO as high quality high-k gate dielectrics. For poly-Si/HfSiO transistors, we have reported over 95% carrier mobility compared to SiO_2.[5] As MG material, Ta and TiN were chosen for N and PMOS transistors, respectively. Ta and TiN were deposited on HfSiO by using an ultra-long-throw (target-to-sample distance of 300mm) UHV sputtering system, which can suppress the sputtering damage to gate dielectrics.

3. Results and discussions

Figure 2 shows C-V characteristics of the MG/HfSiO transistors. We find the gate depletion is completely absent in our MG devices. Effective WFs estimated from the flatband voltage, are 4.3eV (mid gap -0.3eV) for Ta, and 4.9eV (mid gap +0.3eV) for TiN, respectively, including the possible contribution of effect of fixed charges within HfSiO. These values are close to reported ones of 4.2 eV for Ta and 4.7-4.9 eV for TiN on SiO_2.[2,6] Indeed, the 0.1eV difference in WFs between MG on HfSiO and on SiO_2 is likely to be due to fixed charges within HfSiO.

Thermal stability of MG/high-k interface is also very important for device application. Figure 3 shows the change in effective WF and gate leakage current (Ig) for TiN/HfSiO-MOS capacitor after N_2 annealing. The effective WF of TiN is almost stable, and Ig increases only slightly up to 600°C. However, at annealing temperatures higher than 600°C, the effective WF suddenly shifts toward mid gap (4.6eV) and Ig increases by more than two orders of magnitude. These changes in the effective WF and Ig indicate that the quality of HfSiO is degraded by MG/HfSiO interface reaction. Similar change due to annealing above 600°C was also observed for Ta electrode.

By minimizing the sputtering damage and thermal budget, excellent leakage suppression is achieved in our MG/HfSiO transistors. As shown in Fig. 4, the degree of suppression amounts to six orders of magnitude compared to poly-Si/SiO_2 device at identical Tinv. Even with the metal sputtering process, our MG/HfSiO stack shows better leakage suppression than poly-Si/HfSiO sample due to the absence of poly-Si formation process: the former showed two orders of magnitude smaller leakage than the poly-Si/HfSiO transistors under accumulation bias (not shown). Of course, elimination of poly-Si depletion also plays a key role in enhancing the figure-of-merit for leakage reduction under transistors operation. The overall leakage reduction of six-orders-magnitude is a consequence of these two contributions.

Figure 5 shows Id-Vg characteristics of Ta- NMOS and TiN-PMOS transistors with HfSiO. The subthreshold swings were 70 mV/dec for Ta-NMOS and 80 mV/dec for TiN-PMOS, respectively. These values are identical to that of poly-Si/SiO_2 gate stack transistors. Meanwhile, the values of Vth are 0.55V for NMOS and -0.49V for PMOS (channel doping: $1x\ 10^{18}cm^{-3}$) as indicated in Fig. 5. We point out that, by optimizing channel doping, it should be possible to reduce Vth down to ±0.3V.[7]

Figure 6 shows carrier mobility for MG/HfSiO transistors as a function of effective field (Eeff). No

degradation in electron mobility was noted for Ta-NMOS transistors at Eeff of 0.9MV/cm. On the other hand, hole mobility for TiN-PMOS transistors was 60% compared to poly-Si/SiO_2 stack at 0.9MV/cm. Summarizing the observed transistor characteristics, we conclude that our low-damage process approach fo Ta and TiN dual MG CMOS with HfSiO gate dielectrics seems quite successful in realizing future low leakage device, except for the PMOS mobility, which still is lager than previous reported values for MG/high-k transistors

4. Conclusions

We investigated the MG/HfSiO transistors using TiN and Ta for MG. The effective WF of Ta and TiN are 4.3eV and 4.9eV, respectively. We obtained symmetrical Vths under these WFs. The electron and hole mobilities estimated from Ta and TiN gate transistors were 100% and 60% of those for reference SiO_2 transistors. Low leakage current ($1x10^{-3}A/cm^{-2}$) was achieved at Tinv down to 1.7nm. We suggest that HfSiO is one of the candidates for MG/high-k gate transistors.

References

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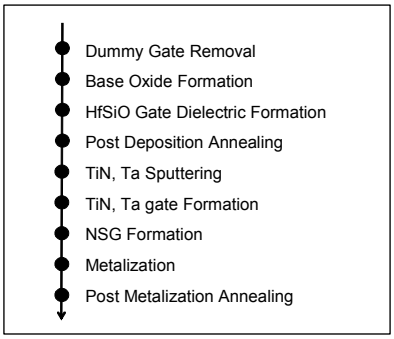

Fig. 1 Process flow of replacement gate transistor fabrication.

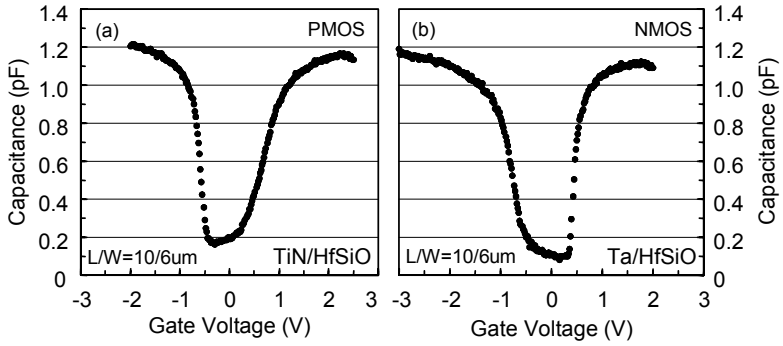

Fig. 2 C-V characteristics of MG/HfSiO-PMOS(a) and -NMOS(b) capacitors. EOT of HfSiO was 1.4 nm.

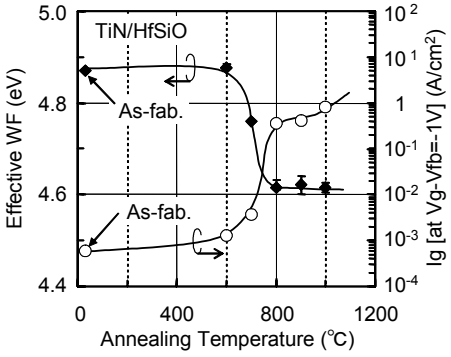

Fig. 3 Thermal stabilities of effective WF and Ig for TiN/HfSiO.

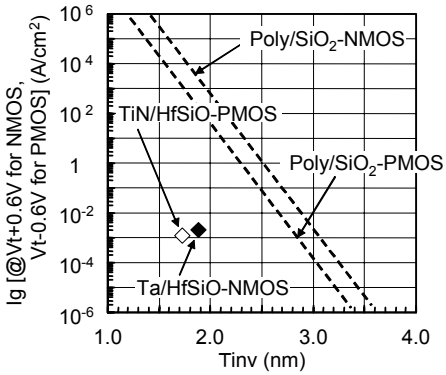

Fig. 4 Ig-Tinv characteristics of Ta and TiN gate transistors.

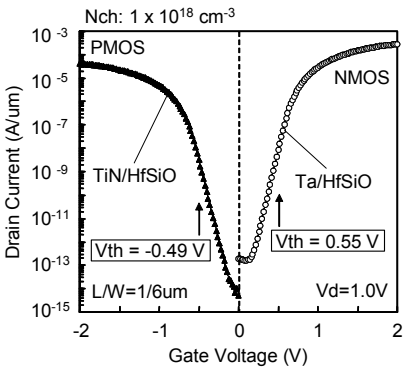

Fig. 5 Id-Vg characteristics of Ta-NMOS and TiN- PMOS transistors.

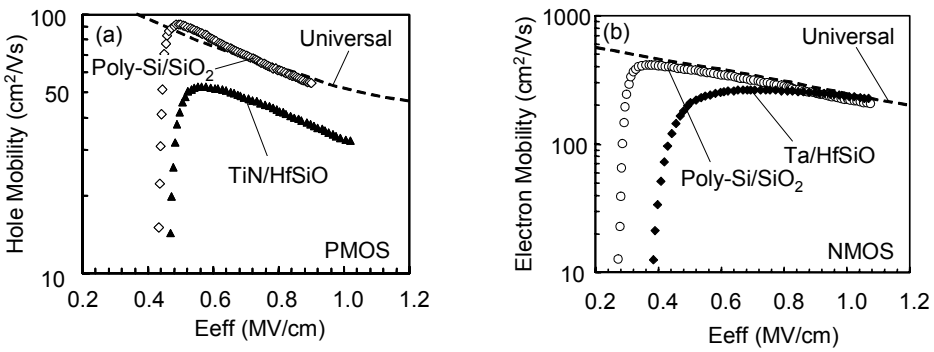

Fig. 6 Hole(a) and electron(b) mobilities of MG/HfSiO and poly-Si/SO_2 transistors .