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Temperature effects of constant bias stress on NFETs with Hf-based gate dielectric

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1. Introduction

High-k dielectrics are known to have high density of preexisting traps [1], which may exhibit reversible trapping/detrapping behavior [2]. Previous works on NFETs with the poly gate electrode and HfSiO gate dielectric have demonstrated that at room temperature a significant portion of the threshold voltage (V_{th}) shift caused by a positive gate bias stress was reversible [2]. On the other hand, at higher temperatures, a so-called "turn-around" V_{th} behavior (when, during the stress, the V_{th} shift changes its sign) under the positive bias stress on NMOSFET with poly/HfO_2 gate stack was reported [3].

In this work, the positive-bias-temperature instability (PBTI) phenomenon and origin of the "turn-around" behavior were studied in NMOS transistors with HfSiO/poly gate stack.

2. Experimental results and discussion

Device Fabrication

The NMOSFETs with the polysilicon or TiN gate electrode and HfSiO gate dielectric were utilized in this study. The MOCVD Hf-silicate film of 4.0 nm was deposited on O_3 cleaned Si-substrate. The XPS analysis showed 4:1 ratio of Hf to Si in the bulk of the film. Nitrogen was incorporated in the dielectric by the NH_3 post-deposition-anneal (PDA) at 700°C for 60 sec.

After the gate patterning, high-k layer was removed with a minimal damage to the extension region. Then, a thin nitride layer (~5nm) was deposited to prevent the process-induced charging damage due to microcontamination of the high-k film [4]. LDD and halo were implanted through the seal nitride and their doses and energies were optimized to ensure a proper overlap of the LDD and gate electrode, and to control o short channel behavior. Then, the oxide spacers were formed followed by the source/drain implantation. The source/ drain activation was performed at 1000°C, 5sec in N_2 ambient. Finally, forming gas anneal was performed at 480°C for 30 minutes after metal patterning.

Results and Discussion

Fig. 1 shows that degradation of the transistor Id-Vg characteristics under the positive gate bias stress (2.2V) strongly depends on the stress temperatures. At room temperature, V_{th} increased monotonically, with no changes in the slopes of the Id-Vg curves, which determined the subthreshold swing values. However, at 150°C, the V_{th} turn-around effect was observed accompanied by a significant subthreshold swing and transconductance degradations.

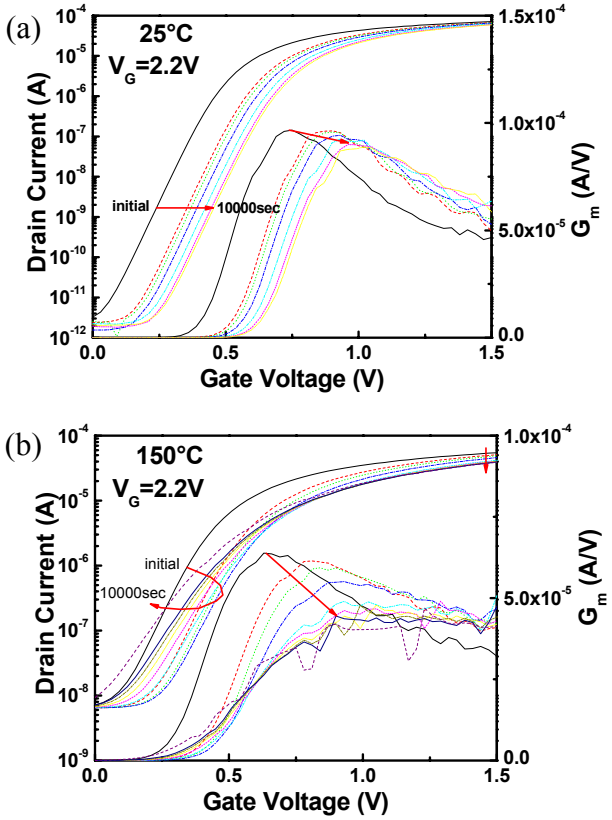

Fig. 1 Id-Vg and G_m changes under positive bias stress (a) at room temperature and (b) at 150°C.

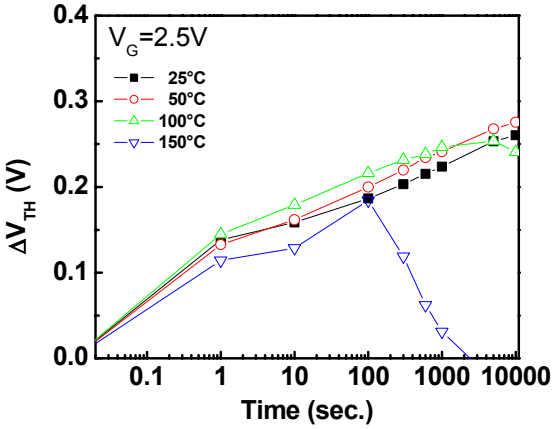

Fig. 2 The time dependence of the V_{th} shift under 2.5V stress at various temperatures

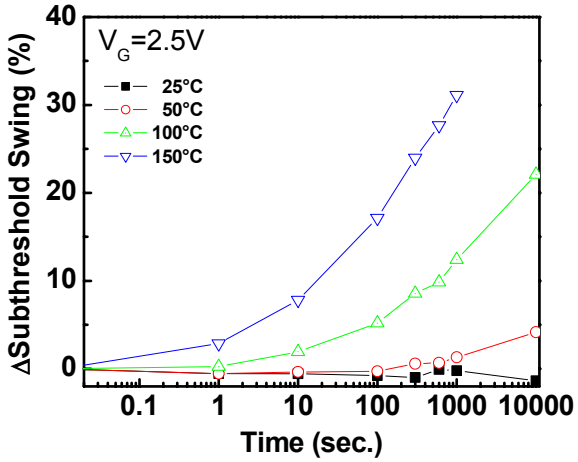

Fig. 3 Subthreshold swing degradation with the Vg=2.5V stress time at different temperatures.

V_{th} changes under 2.5V stress at various temperatures are summarized in Fig. 2. While V_{th} shifts at room temperature and 50°C were very similar, it began to exhibit a turn-around behavior by the end of the 1000 sec stress at 100°C, this effect being more pronounced during the 150°C stress. It indicates that the positive charging gradually increased the stress temperature. Subthreshold swing showed the dependence of its degradation on temperature even more clearly (Fig. 3) and this degradation is not reversible (data not shown).

It is interesting to notice that the TiN gate NMOSFET did not exhibit the V_{th} turn-around behavior at high temperatures (Fig. 4), while the subthreshold swing degradation was relatively small (less than 10%) compared to the poly-Si electrode samples.

Based on these results, we speculate that significant amount of holes were generated by impact at the poly-Si/HfSiO interface by the hot-electrons injected into the dielectric during the positive gate bias stress, and some hole could be injected back in the dielectric and, subsequently, trapped there [5].

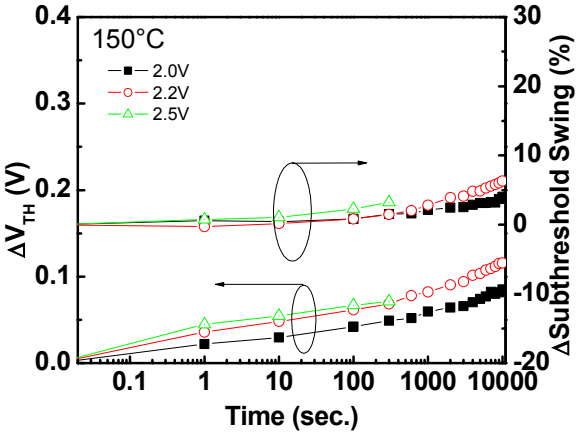

Fig. 4 The stress time dependence of the V_{th} shift and subthreshold swing degradation in TiN/HfSiO gate stack at different stress voltages at 150°C. In the 2.5V stress, a breakdown occurred around 300sec.

The hole diffusion through the dielectric could be enhanced by temperature. The holes trapped near the interface with the Si substrate produce greater V_{th} shift and might be responsible for the degradation of subthreshold swing and transconductance. Additional possibility which is currently under investigation is the variation of the physical quality of the interfacial region for polysilicon vs. metal gate electrode.

This suggestion is further supported by the data on the gate leakage variation in the poly-Si and TiN gate stacks during the stress, Fig. 5. While there were no significant changes at room temperature stress, the gate leakage gradually increased by almost 4 orders of magnitude during the 150°C stress. Taking into account that the TiN electrode sample did not exhibit any gate current increase up to the breakdown, we suggest that the trapping of the gate electrode-related holes in the interfacial layer at the high-k/Si-substrate interface might be responsible for the observed gate leakage current increase in the device with the poly-Si gate electrode.

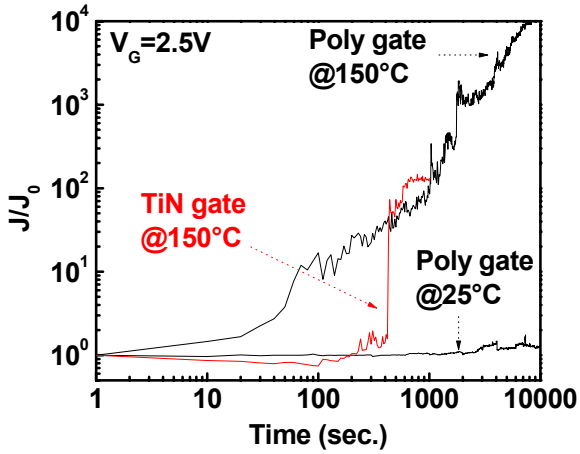

Fig. 5 Relative increase of the gate leakage current during the 2.5V stress at RT and 150°C in devices with the poly-Si and TiN gate electrodes (J_0 is initial gate leakage current).

3. Conclusions

The V_{th} turn around phenomenon, accompanied by decreasing transconductance and rising gate leakage current, was observed in the NMOSFETs with the poly-Si/HfSiO gate stack under the positive gate bias high temperature stress. It is proposed that the generation of holes in the poly-Si electrode and their subsequent diffusion in the dielectric film and trapping at the high-k/Si-substrate interface might be responsible for the degradation of the transistor characteristics. This hole induced degradation may further complicate integration of the poly-Si gate electrode with the high-k dielectrics

References

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