Charge Trapping Characteristics of Hafnium Based High-κ Dielectrics with Various Metal Electrodes

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1. Introduction
High-κ dielectrics in conjunction with metal gates are proposed to be incorporated in planar CMOS to facilitate scaling trends below the 65 nm node. However this can be realized only when the reliability of these advanced gate stacks are thoroughly characterized and degradation mechanisms well understood. It was proposed earlier in a charge trapping study [1] that the electrical stress can generate electron traps in hafnium based high-κ dielectrics. On the other hand, both the pulse and conventional DC \( I_{D-V_S} \) measurements [2-5] did not show noticeable stress-induced trap generation and point to the contribution of the pre-existing electron traps as the cause of transistor parameter instability. Clearly, further analysis of the advanced gate stacks is needed to evaluate the process-structure-property interrelationship in high-κ stacks. In this study, various high-κ/metal gate stacks were studied to address the dependence of charge trapping characteristics on the composition of the hafnium based high-κ dielectrics [hafnium silicate (HfSiO\(_x\)) vs. hafnium oxide (HfO\(_2\))], and the method of the metal gate deposition process: atomic layer deposition (ALD) vs. physical vapor deposition (PVD).

2. Experimental Procedure
Planar CMOS transistors with physical channel lengths (85 nm – 20 μm) utilizing hafnium based high-κ dielectrics and different metal gate electrodes were fabricated using the standard transistor process (gate first), with a 1000°C/10 sec S/D dopant activation, and the final forming gas anneal at 480°C for 30 minutes in N\(_2\)/H\(_2\). This study focused on charge trapping studies of two gate stack material sets: (a) HfSiO\(_x\) vs. HfO\(_2\) films processed by chemical vapor deposition (CVD) with TaSiN electrodes and (b) TiN processed by ALD vs. PVD on HfSiO\(_x\) films. For electrical evaluation, a CVS was used with a~1 V/10 seconds stress applied after each positive stress cycle. Afterward, a threshold voltage measurement (i.e., linear regime \( I_{D-V_S} \)) or a charge pumping measurement with fixed amplitude and base voltage, were performed at several different frequencies [5]. Complementing the charge trapping studies were a battery of physical (C-V, I-V, \( I_{D-V_S} \), carrier mobility extraction) and physical (cross-section HRTEM, STEM-EELS) characterization.

3. Results and Discussion:
MOCVD HfO\(_2\) vs. HfSiO\(_x\) with TaSiN electrodes:
Figure 1 is the Fixed-Amp. CP data of HfO\(_2\) and HfSiO\(_x\) thin films (40 Å) processed by CVD, on the ozone treated chemical oxide silicon surface. The high frequency \( N_a \) value for both these stacks are similar, indicating that the interface structure (bottom interfacial oxide with Si channel) for the stacks is identical. However, the higher \( N_a \) values for lower CP frequencies (meaning probing deeper into the bulk of the gate stack and/or energetically deeper electron traps) are indicative of higher density of trap states for HfO\(_2\) dielectrics compared to HfSiO\(_x\). This may be associated with higher Hf content in the HfO\(_2\) compared to HfSiO\(_x\). It is noteworthy that there is no indication of trap generation by the stress in the HfSiO\(_x\) stacks. A very similar \( V_{t} \) time dependence in the subsequent stress cycles (which include the electron detrapping with –1V/10 sec gate bias) (Figure 2) corroborates the suggestion that there is no significant electron trap generation in this system. Although there appears to be a certain trap generation in the HfO\(_2\) samples probed with the CP technique, a numerical estimate indicates that its effect on the \( V_{t} \) values is rather small and might not be noticeable in the \( V_{t} \) stress time dependence (Figure 2). The electron trap density in the HfO\(_2\) stack with a TaSiN electrode is higher than in the HfSiO\(_x\) one, as follows from the fast transient analysis, Figure 3. At the same time, the gate leakage current in inversion is also higher in HfO\(_2\) stack of the same physical thickness as HfSiO\(_x\) indicating the inferior quality of the latter. This conclusion is further supported by the lower carrier mobility in the HfO\(_2\) transistors comparing to HfSiO\(_x\) (not shown). Comparing these gate stacks, one may conclude that, although HfO\(_2\) is preferable from a scaling standpoint, it may be problematic based on the charge trapping rate. Thus, greater density of the pre-existing electron traps and their propensity to generate additional
traps by stress, may make the HfO₂ material less attractive as a gate dielectric.

**ALD vs. PVD TiN on HfSiOₓ**

The Fixed-Amplitude Charge Pumping data collected in the gate stacks with ALD and PVD processed TiN on HfSiOₓ thin films (40 Å) on ozone chemical oxide treated silicon are presented in Figure 4. The stronger N<sub>t</sub> dependence on the CP frequency in the PVD samples indicates that more trap states may be present deeper in the bulk of the gate stack (and/or these traps have deeper energy levels). Again, there is no indication of generation of traps with the stress in the HfSiOₓ dielectric. This is consistent with the observation of complete recovery of V<sub>t</sub> after the application of the de-trapping bias for both the ALD and PVD TiN samples, as shown in Figure 5. Difference between the high frequency N<sub>t</sub> values in these gate stacks clearly indicates that the metal electrode deposition process has significant impact on the bottom interfacial layer: N<sub>t</sub> changes with the gate electrode process although both stacks received an identical pre-deposition treatment and high-κ film deposition. To study the physical properties of the bottom interface, cross-section HRTEM images with EELS chemical scans were collected, Figure 6. The data analysis confirms that the interfacial oxide thickness for ALD TiN is greater than in the PVD case. This may be due, in part, to the higher process temperature with sufficient partial pressure of oxygen for ALD TiN (∼545°C) compared to PVD TiN (∼room temperature) that also may result in higher oxygen content and therefore greater band gap in the former [6]. The superior quality of the ALD TiN stack compared to the PVD TiN is also reflected in a comparison of the gate leakage currents under the substrate injection condition (J<sub>s</sub> @ 1.5 V for ALD TiN = 5x10<sup>−3</sup> A/cm² and PVD TiN = 5x10<sup>−2</sup> A/cm²). It is therefore apparent that although the PVD gate electrodes may not degrade the electrical quality of the dielectric films (no trap generation with stress), the shear variance in the electrode processing conditions may have significant impact on the structure and property of the bottom interfaces in the advanced gate stack.

3. Summary

Scaled CMOS transistors with HfO₂ and HfSiOₓ dielectrics and TaSiN and ALD and PVD TiN metal gates were characterized. From a device performance perspective, it was concluded that the HfSiOₓ films demonstrated certain advantages over the HfO₂. The TiN PVD gate electrode was not found to degrade the bulk HfSiOₓ dielectrics properties, however, it seems to affect the quality of the bottom interfacial layer. This points to a potentially significant impact of the gate electrode processing on the gate stack bottom interface.

References