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Charge Trapping Characteristics of Hafnium Based High-κ Dielectrics with Various Metal Electrodes

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1. Introduction

High-κ dielectrics in conjunction with metal gates are proposed to be incorporated in planar CMOS to facilitate scaling trends below the 65 nm node. However this can be realized only when the reliability of these advanced gate stacks are thoroughly characterized and degradation mechanisms well understood. It was proposed earlier in a charge trapping study [1] that the electrical stress can generate electron traps in hafnium based high-κ dielectrics. On the other hand, both the pulse and conventional DC I_d-V_g measurements [2-5] did not show noticeable stress-induced trap generation and point to the contribution of the pre-existing electron traps as the cause of transistor parameter instability. Clearly, further analysis of the advanced gate stacks is needed to evaluate the process-structure-property interrelationship in high-κ stacks. In this study, various high-κ/metal gate stacks were studied to address the dependence of charge trapping characteristics on the composition of the hafnium based high-κ dielectrics [hafnium silicate ($HfSiO_x$) vs. hafnium oxide (HfO_2)], and the method of the metal gate deposition process: atomic layer deposition (ALD) vs. physical vapor deposition (PVD).

2. Experimental Procedure

Planar CMOS transistors with physical channel lengths (85nm – 20 μm) utilizing hafnium based high-κ dielectrics and different metal gate electrodes were fabricated using the standard transistor process (gate first), with a 1000^{o}C/10 sec S/D dopant activation, and the final forming gas anneal at 480^{o}C for 30 minutes in N_2/H_2. This study focused on charge trapping studies of two gate stack material sets: (a) $HfSiO_x$ vs. HfO_2 films processed by chemical vapor deposition (CVD) with TaSiN electrodes and (b) TiN processed by ALD vs. PVD on $HfSiO_x$ films. For electrical evaluation, a CVS was used with a–1 V/10 seconds stress applied after each positive stress cycle. Afterward, a threshold voltage measurement (i.e., linear regime I_d–V_g) or a charge pumping measurement with fixed amplitude and base voltage, were performed at several different frequencies [5]. Complementing the charge trapping studies were a battery of electrical (C-V, I-V, I_d-V_g, carrier mobility extraction) and physical (cross-section HRTEM, STEM-EELS) characterization.

3. Results and Discussion:

MOCVD HfO_2 vs. HfSiOx with TaSiN electrodes:

Figure 1 is the Fixed-Amp. CP data of HfO_2 and $HfSiO_x$ thin films (40 Å) processed by CVD, on the ozone treated chemical oxide silicon surface. The high frequency N_{it} value

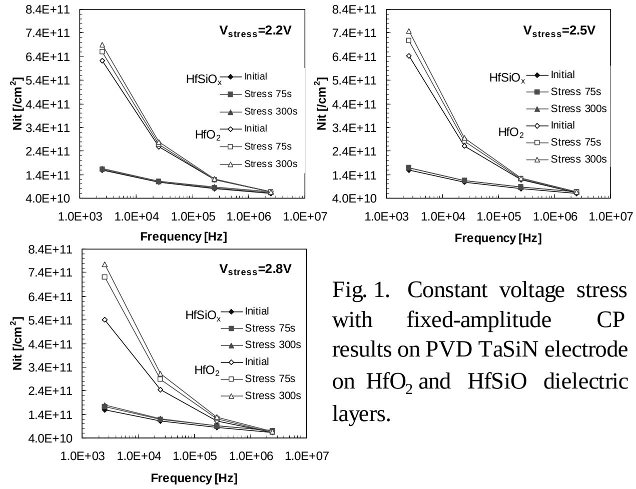


Fig. 1. Constant voltage stress with fixed-amplitude CP results on PVD TaSiN electrode on HfO_2 and HfSiO dielectric layers.

for both these stacks are similar, indicating that the interface structure (bottom interfacial oxide with Si channel) for the stacks is identical. However, the higher N_{it} values for lower CP frequencies (meaning probing deeper into the bulk of the gate stack and/or energetically deeper electron traps) are indicative of higher density of trap states for HfO_2 dielectrics compared to $HfSiO_x$. This may be associated with higher Hf content in the HfO_2 compared to $HfSiO_x$. It is noteworthy that there is no indication of trap generation by the stress in the HfSiOx stacks. A very similar V_t time dependence in the subsequent stress cycles (which include the electron de-trapping with –1V/10 sec gate bias) (Figure 2) corroborates the suggestion that there is no significant electron trap generation in this system. Although there appears to be a certain trap generation in the HfO_2 samples probed with the CP technique, a numerical estimate indicates that its effect on the V_t values is rather small and might not be noticeable in the V_t stress time dependence (Figure 2). The electron trap density in the HfO_2 stack with a TaSiN electrode is higher than in the $HfSiO_x$ one, as follows from the fast transient analysis, Figure 3. At the same time, the gate leakage current in inversion is also higher in HfO_2 stack of the same physical thickness as $HfSiO_x$ indicating the inferior quality of the latter. This conclusion is further supported by the lower carrier mobility in the HfO_2 transistors comparing to $HfSiO_x$ (not shown). Comparing these gate stacks, one may conclude that, although HfO_2 is preferable from a scaling standpoint, it may be problematic based on the charge trapping rate. Thus, greater density of the pre-existing electron traps and their propensity to generate additional

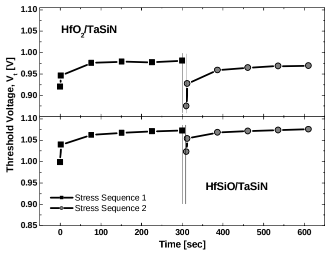


Fig. 2. Time dependence of the threshold voltage shift of the TaSiN electrode on HfO_2 and HfSiOx during CVS. At the end of the stress cycle, a discharge of -1 V/10 sec was done , and the stress cycle was repeated.

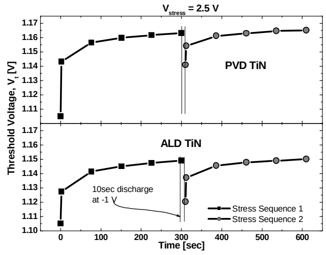


Fig. 5. Time dependence of the threshold voltage shift of the ALD and PVD TiN electrode on HfSiOx during CVS. At the end of the stress cycle, a discharge of -1 V/10 sec was done , and the stress cycle was repeated.

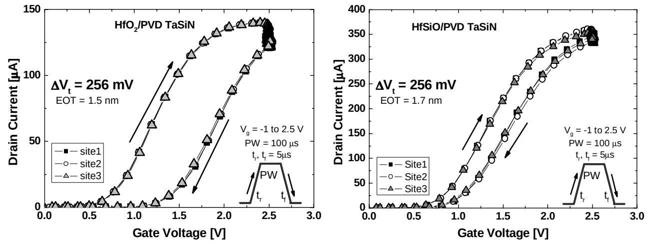


Fig. 3. Single Pulse measurements in HfO_2 v. $HfSiO_x$ gate stack.

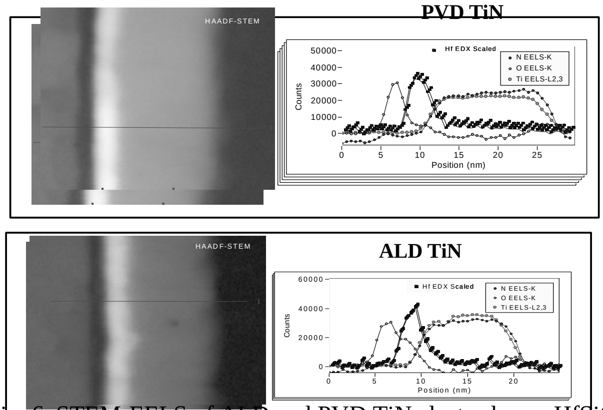
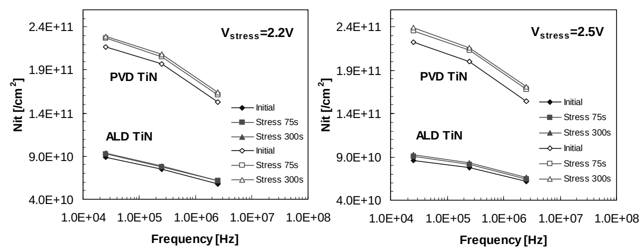


Fig. 6. STEM-EELS of ALD and PVD TiN electrodes on HfSiOx dielectric layers.

traps by stress, may make the HfO_2 material less attractive as a gate dielectric.

ALD vs. PVD TiN on HfSiOx:

The Fixed-Amplitude Charge Pumping data collected in the gate stacks with ALD and PVD processed TiN on HfSiOx thin films (40 Å) on ozone chemical oxide treated silicon are presented in Figure 4. The stronger N_{it} dependence on the CP frequency in the PVD samples indicates that more trap states may be present deeper in the bulk of the gate stack (and/or these traps have deeper energy levels). Again, there is no indication of generation of traps with the stress in the $HfSiO_x$ dielectric. This is consistent with the observation of complete recovery of V_t after the application of the de-trapping bias for both the ALD and PVD TiN samples, as shown in Figure 5. Difference between the high frequency N_{it} values in these gate stacks clearly indicates that the metal electrode deposition process has significant impact on the bottom interfacial layer: N_{it} changes with the gate electrode process although both stacks received an identical pre-deposition treatment and high-κ film deposition. To study the physical properties of the bottom interface, cross-section HRTEM images with EELS chemical scans were collected, Figure 6. The data analysis confirms that the interfacial oxide thickness for ALD TiN is greater than in the PVD case. This maybe due, in part, to the higher process temperature with sufficient partial pressure of oxygen for ALD TiN (~545^{o}C) compared to PVD TiN (~ room temperature) that also may result in higher oxygen content and therefore greater band gap in the former [6]. The superior quality of the ALD TiN stack compared to the PVD TiN is also reflected in a comparison of the gate leakage currents under the substrate injection condition (J_g @ 1.5 V for ALD TiN = $5x10^{-3}$ A/cm^2 and PVD TiN= $5x10^{-2}$ A/cm^2). It is therefore apparent that although the PVD gate electrodes may not degrade the electrical quality of the dielectric films (no trap generation with stress), the sheer variance in the electrode processing conditions may have significant impact on the structure and property of the bottom interfaces in the advanced gate stack.



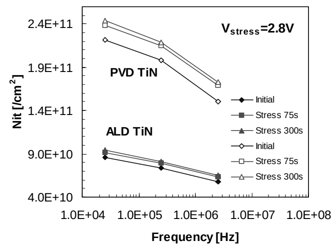


Fig. 4. Constant voltage stress with fixed-amplitude CP results on ALD and PVD TiN electrodes on HfSiO dielectric layers.

3. Summary

Scaled CMOS transistors with HfO_2 and $HfSiO_x$ dielectrics and TaSiN and ALD and PVD TiN metal gates were characterized. From a device performance perspective, it was concluded that the $HfSiO_x$ films demonstrated certain advantages over the HfO_2. The TiN PVD gate electrode was not found to degrade the bulk $HfSiO_x$ dielectrics properties, however, it seems to affect the quality of the bottom interfacial layer. This points to a potentially significant impact of the gate electrode processing on the gate stack bottom interface.

References

[1] R. Degraeve, et, al., *IEDM*, p. 935, Dec. 2003
[2] C.D. Young, et al., *IRPS*, p. 597, March 2004
[3] Bersuker, et al., *presented at the Spring MRS*, 04/2004
[4] Bersuker, et al., *submitted to ESREF 2004*
[5] C.D. Young, et al., *to be presented at WoDiM*, Ireland, 06/2004
[6] Bersuker et al., *to be presented at IWDTF*, Tokyo, 06/2004