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Dependences of Device Performances on Interfacial Layer Materials of High-k MISFETs due to Wave Function Penetration into Gate Dielectrics

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Abstract
In this paper it is shown that tunneling probability of electrons (TP), capacitance equivalent oxide thickness (CET), and propagation delay time (τ_{pd}) of high-k MISFETs are strongly affected by interfacial layer (IL) materials in the case that wave function penetration into gate dielectrics is taken into consideration. Using reported barrier heights and effective masses, these parameters in MISFETs with HfO_2/IL stacked gate dielectrics with interfacial layer of SiO_2, Si_3N_4, Al_2O_3, Ta_2O_5, and $SrTiO_3$ are quantitatively studied.

1. Introduction
The trend toward miniaturization has resulted in thinning of gate dielectrics, and according to the ITRS, they should be less than 1 nm within 3 years. In order to avoid the drastic leakage current increase that is inherent in such thin SiO_2 gate dielectrics, high-k materials for gate dielectrics are being intensively investigated [1]. Considering such a small thickness of dielectrics, inversion layer thickness is no longer negligible. So far, materials and fabrication method of IL have been studied mainly in terms of inversion layer mobility just below them. In this report, we quantitatively investigated the influence of the IL material on inversion layer thickness using numerical simulation taking wave function penetration into gate dielectrics into consideration, and found that the thickness is strongly affected by IL materials in stacked gate dielectric MISFETs, resulting in large τ_{pd} dependence on the materials.

2. Model in Simulation
Depth of charge centroid, i.e., inversion layer thickness (T_{inv}) and TP of carriers, which is considered to be proportional to gate leakage current, were simulated at $N_{inv} = 5x10^{12}$ cm^{-2} (carrier density around $V_G = V_{DD}$ [2]) for a stacked gate dielectric structure shown in Fig. 1. We used a model based on the WKB approximation and required wave functions to exponentially decay deep both in substrate and gate dielectrics and wave functions and their derivatives to be continuous at every interface. The substrate was assumed to be Si (100) substrate with a uniform impurity concentration of $1x10^{18}$ cm^{-3}. Electrical potential in the substrate was approximated by a triangular potential and only the lowest sub-band was taken into consideration. Neither charge inside the gate dielectrics nor at the gate dielectric/substrate interface was assumed to exist. The effective masses in Si substrate were set to $m_l = 0.98m_0$, $m_t = 0.19m_0$ and $m_{LH} = 0.16m_0$, $m_{HH} = 0.49m_0$ for electrons and holes, respectively [3], where m_0 is the free electron mass. The assumed values of dielectric constant (k), barrier height (ϕ_B), and effective mass (m_{eff}) of carriers in supposed ILs are summarized in Table I. HfO_2 interfacial layer corresponds to a gate dielectric of HfO_2 monolayer. The temperature was assumed to be 300K and the Boltzmann statistics were used in calculations of thermodynamical average.

3. Results and Discussion
Wave functions of electrons for various interfacial layers (Fig. 2) show that their shapes are almost equal for SiO_2, Si_3N_4, and Al_2O_3 IL and HfO_2 monolayer. The reason for this is that ϕ_B in these cases are so much higher than in the other 2 cases that it is possible to physically approximate ϕ_B to be infinitely high. The penetration of wave function into gate dielectric is obviously larger in the Ta_2O_5 IL and even larger in the $SrTiO_3$ IL, resulting in shallower T_{inv}. Table II summarizes thermodynamical average of energy measured from E_C at the substrate surface, T_{inv}, and TP for electrons. Fig. 3 shows the results summarized in Table II in TP versus CET plane, where CET = T_{inv}x3.9/11.9+EOT. A trend line for SiO_2 IL with HfO_2 layers of various thickness is also shown. Reduction in TP can be divided into 2 parts, which are shown in Fig. 3 for comparison between SiO_2 and $SrTiO_3$ IL cases as an example. The part A represents the reduction in TP due to the increase in dielectric constant and thickness of IL, whereas the part B is the genuine effect of decrease in T_{inv}. Fig. 4 shows the dependences of A and B on IL materials as compared with the SiO_2 IL case. In the $SrTiO_3$ IL case, TP of electron is reduced by more than 2 orders of magnitude due to a change in T_{inv}.
Equivalent analysis for holes was also carried out. Fig. 5 shows wave functions of holes for various interfacial layers. Contrary to the case of electrons (Fig. 2), the shapes of wave functions are almost independent of IL materials. ϕ_B for holes are so high that it is possible to physically approximate ϕ_B to be infinitely high for all materials.
Studies on τ_{pd} were carried out for 35 nm gate length devices with stacked gate dielectric structures shown in Fig. 1 with various ILs using a device model [10]. As for mobility of carriers, that in SiO_2/Si systems was used for all IL devices in order to concentrate on the effect of the change in T_{inv}. The results are shown in Fig. 6 with filled symbols. In the lowest order approximation, τ_{pd} is proportional to $C_{tot}V_{DD}/I_D$, where C_{tot}, V_{DD}, and I_D are total capacitance, power supply voltage, and drain current, respectively, and C_{tot} consists of C_{ch}, C_{ov}, C_{fringe}, and C_j, which are channel, overlap, fringe, and junction capacitance, respectively. Hence, τ_{pd} is proportional to $1+3xC_{ov}/C_{ch}+3xC_{fringe}/C_{ch}+C_j/C_{ch}$, where the Miller effect is taken into consideration. Therefore, a large increase in C_{ch} with the T_{inv} reduction leads to the effective decrease in τ_{pd}. It should be noted that changing IL to higher-k material induces changes not only in CET but also in fringe capacitances. In order to extract the influence of the latter effect, simulations were carried out without changing T_{inv}, i.e., with fixed CET, the results of which are also shown in Fig. 6. In the $SrTiO_3$ IL case τ_{pd} was reduced by 0.3 ps as compared with the SiO_2 IL case and 0.14 ps of the reduction is due to a reduction in T_{inv}.
Finally, dependence of T_{inv} in nMISFET on the physical thickness of IL was studied. Fig. 7 shows that T_{inv} in $SrTiO_3$ IL case, for example, gradually diminishes along with an increase in its physical thickness and saturates when it surpasses the penetration depth (≈ 4 nm, EOT of only 0.09 nm).

4. Summary and Conclusion
It has been shown that an influence of barrier height and effective mass of carriers in interfacial layer on

device performances is quite large. Materials with low barrier heights and high dielectric constants can be promising candidates for interfacial layer of gate dielectrics with a thickness of less than 1 nm.

References

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Table I Dielectric constant, barrier height, and effective mass of supposed materials in the simulation.

Interfacial Layer	k	Electrons		Holes	
		ϕ_B (eV)	m_{eff} (m_0)	ϕ_B (eV)	m_{eff} (m_0)
SiO_2	3.9	3.5[6]	0.5[8]	4.4[6]	0.32[9]
Si_3N_4	7.8	2.4[6]	0.5[9]	1.8[6]	0.41[9]
Al_2O_3	10	2.8[6]	0.2	4.9[6]	0.2
Ta_2O_5	28[4]	0.3[6]	0.2	3.0[6]	0.2
$SrTiO_3$	175[5]	0.23[7]	0.2	1.97[7]	0.2
HfO_2	20	1.5[6]	0.2[9]	3.4[6]	0.2

Table II Thermodynamical average of energy measured from E_C at the substrate surface, depth of charge centroid, and tunneling probability for electrons.

Interfacial Layer	Energy (eV)	Centroid (nm)	Tunneling Probability
SiO_2	0.110	1.32	1.04×10^{-10}
Si_3N_4	0.109	1.30	1.87×10^{-11}
Al_2O_3	0.105	1.22	3.05×10^{-11}
Ta_2O_5	0.087	0.78	8.51×10^{-11}
$SrTiO_3$	0.084	0.61	2.63×10^{-14}
HfO_2	0.101	1.13	5.62×10^{-12}

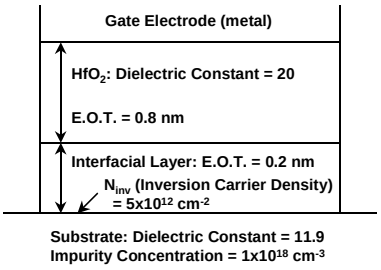

Fig. 1 Stacked gate dielectric structure used in the simulation.

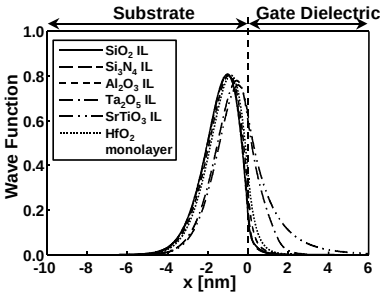

Fig. 2(a) Wave functions of electrons in 2-fold valleys.

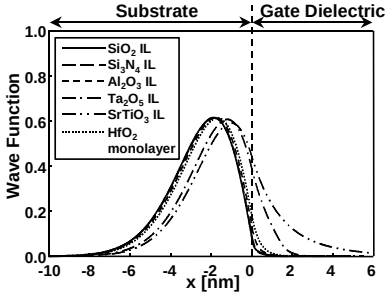

Fig.2(b) Wave functions of electrons in 4-fold valleys.

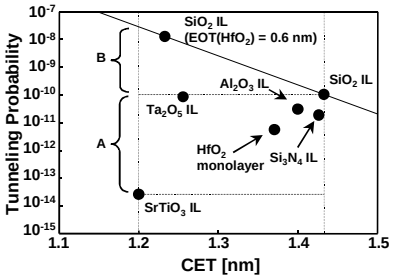

Fig. 3 Simulated results in tunneling probability versus CET plane. A trend line for SiO_2 IL with HfO_2 layers of various thickness is also drawn.

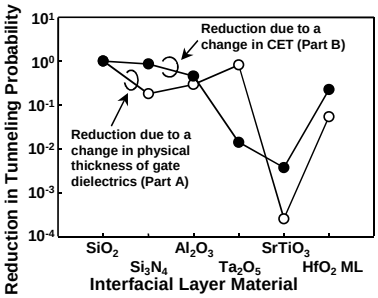

Fig. 4 Reduction in tunneling probability for various interfacial layer cases.

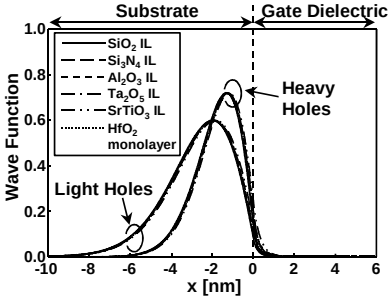

Fig. 5 Wave functions of holes.

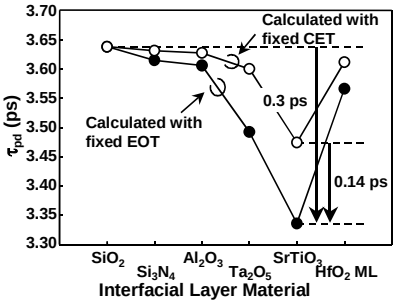

Fig. 6 Dependences of propagation delay time on interfacial layer materials.

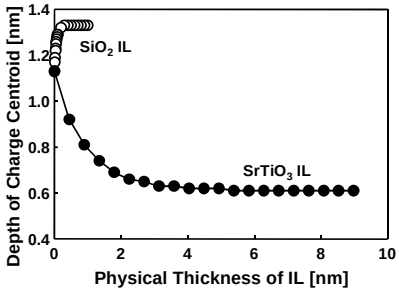

Fig. 7 Dependences of T_{inv} in nMISFET on physical thickness of IL.