Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 178-179

A-5-4

A New Well Capacity Adjusting Scheme for High Sensitivity, Extended Dynamic Range CMOS Imaging Pixel Sensors

Cheng-Hsiao Lai, Yueh-Ping Yu and Ya-Chin King

Microelectronic Laboratory, Semiconductor Technology Application Research (STAR) Group,
Department of Electrical Engineering, National Tsing-Hua University, Hsin-Chu 300, Taiwan, R.O.C.
Phone/Fax: +886-3-5715131-4034/+886-3-5721804, E-mail: cclai@well.ee.nthu.edu.tw

1. Introduction

CMOS image sensors, compared with CCD, becomes popular due to their low voltage supply, low power consumption, and compatibility with standard CMOS processes [1]. However, the advances in process technology will result in dramatic increase dark current and decrease sensitivity [2] and therefore narrowed its application. Although the dark current can be reduced through modification of CMOS process [3] and a 4-T pixel with transfer gate was proposed to improve sensitivity [4]. The dynamic range of CMOS APS is still more than an order of magnitude smaller than that of CCD. A 3-T active pixel configuration employing a photogate (PG) combining with a photodiode (PD) as shown in Fig.1 was proposed to reduce dark signal. However, such configuration will suffer lower operation speed and complicated peripheral circuit. In this work, we revisit this cell fabricated by standard 0.25-μm CMOS logic process. A new operation scheme with well capacity adjusting without lowing frame rate is proposed to extend dynamic range as well as improve its sensitivity.

2. Pixel Structure and New Operation Scheme

Fig.2 shows the optical response of the proposed pixel. When PG is biased at a constant voltage of 3.3V, the maximum detectable illumination is higher than that of PG=0V due to its lower sensitivity. At PG=3.3V, the well capacity of photo-sensing area is equivalent to C_{PD}+C_{PG} (C_{PD}: n^+/p-well junction capacitance, C_{PG}: gate dielectric capacitance), and as PG=0V, well capacity reduces to C_{PD}, as shown in fig3. Therefore, the lower charge conversion gain consequently lower the sensitivity and higher dynamic range is obtained with PG=3.3V. The well capacity can be adjusted to meet our application by controlling PG voltage.

The timing diagram of the proposed new operation scheme is illustrated in fig.4. During integration period, the PG will be switched to 0V in a regular time period (t1) and then returned to V_{PG_H}. Fig.5 shows the measurement result of the proposed new operation scheme, where V_{PG_H} =3.3V. The new operation scheme does not affect the output characteristics at low illumination intensity; however, if the illumination is high enough, the photo-sensing node will be pull up to a fixed voltage when PG is from 0V return to 3.3V. This is owing to that the photo-generated electrons which are stored at C_{PG} is transferred to C_{PD} during PG=0V and then be returned to the situation of PG=V_{PG_H}. If the total stored photo-generated electrons exceed the well capacity of C_{PD}, then, the excess electrons will overflow to the substrate or adjacent pixel during PG=0V, and subsequently return to the situation of well capacity is C_{PD}+C_{PG} during PG=V_{PG_H}. Hence, this new well capacity adjusting scheme is expected to extend the dynamic range.

3. Sample Fabrication and Measurement Condition

The CMOS active pixel sensor was fabricated by the TSMC silicided 0.25-μm standard CMOS logic process and operated at 3.3V power supply. The pixel size and fill factor are 7.5x7.5μm^2 and 49% respectively. A 3200K tungsten-halogen lamp and integration sphere were used to provide uniform source of illumination. Besides, the high level of photogate voltage (V_{PG_H}) is varied from 1.8V to 3.3V and the reset pulse low level is set at 0.4V to prevent the blooming effect during the well capacity adjusting period.

4. Experimental Results & Discussions

The measured transferred curve between output and illumination with varied t2 and fixed t1 is shown in fig. 6. It is demonstrated that the maximum detectable illumination can be extended over 10X by adjusting t2. This output transferred curve is similar to result of combining two frames with different integration time of t_I-t2 and t2. The smaller t2 the higher dynamic range is. Fig.7 compares the transfer curves of various t1 with fixed t2. The results show that, the output characteristics are independent of t1. Fig.8 illustrates the optical response for different area ratio of PG to PD. Larger PG to PD area ratio provides higher maximum detectable illumination but suffers the disadvantages of smaller sensitivity at low illumination intensity due to the larger equivalent capacitance. The dynamic range and sensitivity of this cell can be tuned by simply adjusting the V_{PG_H}. As the V_{PG_H}-V_{th_M1} (threshold voltage of M1) becomes smaller than the PD reset level, then, the potential barrier beneath PG is higher than PD and the photo-generated electrons are first stored at the PD region. Under such condition, the sensitivity is the same as the case when PG=0V, until the potential barrier of PD is equal to PG, hereafter, the operation is the same as that of PG=3.3V, as shown in fig.9. Fig.10 shows the dependence of sensitivity and maximum detectable illumination on V_{PG_H}. The maximum detectable illumination can be extended by increasing V_{PG_H}, however the sensitivity maintains at a relative high level compared with conventional 3T_PD cell, if V_{PG_H}<2.8V. The performance comparison of the proposed cell with new operation scheme and conventional 3T_PD cell are summarized in Table I.

5. Conclusions

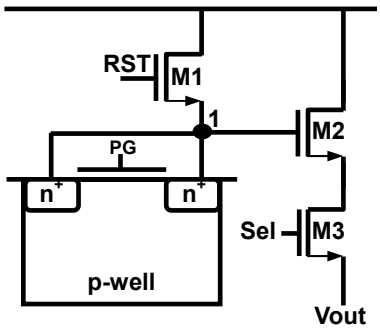
A novel CMOS photon-sensing area with new operation scheme was proposed to extend dynamic range. The imaging sensitivity can be improved through optimizing the PG to PD area ratio and the bias pulse high level. The experimental results demonstrate the pixel can achieve both high sensitivity at low illumination and extended dynamic range for high illumination.

Acknowledgement

The authors would like to acknowledge National Science Council and Chip Implementation Center of the Republic of China for supporting this work.

References

[1] E. Fossum, Proc. SPIE, vol.1900, p.2-14, 1993
[2] H. Wong, IEEE T-ED, Vol. 43, p.2134-2141, 1996.
[3] Ho-Ching Chien et a.l, IEDM Tech. Dig., pp.813-816, 2002
[4] M. Kyomasu,IEEE JSSC,vol. 26,p1116-1122,1991
[5] Hsiu-Yu Cheng et al., IEEE T-ED, vol.50, p.91-95, 2



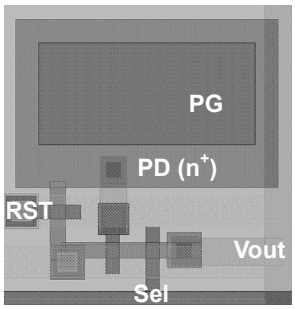


Fig.1 Circuit schematic and layout of the proposed CMOS image sensor cell.

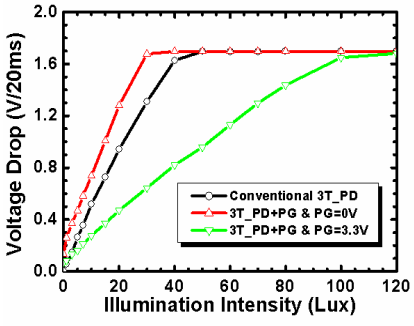


Fig.2. Output characteristics of the proposed pixel with different PG bias.

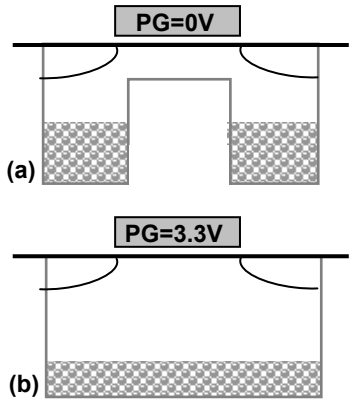


Fig.3. Operation of the proposed pixel (a) PG=0V (b) PG=3.3V

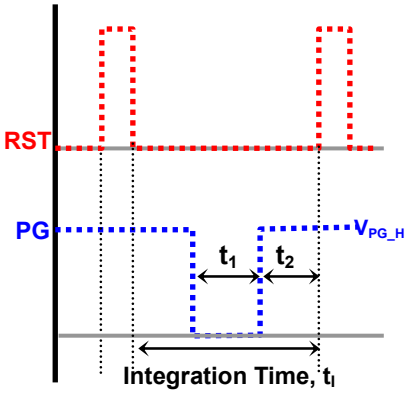


Fig.4 Operation timing diagram of the proposed pixel with well capacity adjusting.

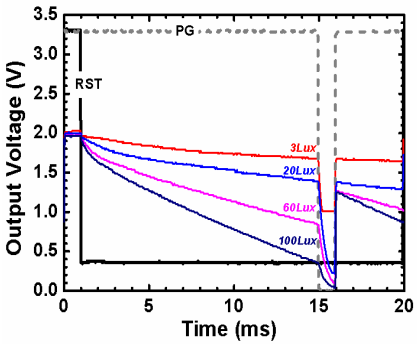


Fig.5. Measurment result of the proposed pixel with well capacity adjusting.

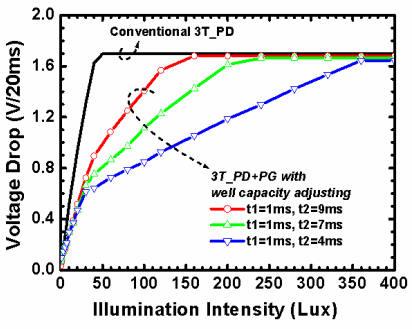


Fig.6. Output characteristics of the proposed pixel with well capacity adjusting with various t2 periods.

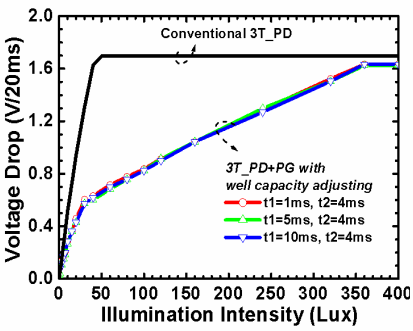


Fig.7. Output characteristics of the proposed pixel with well capacity adjusting with perious t1 periods.

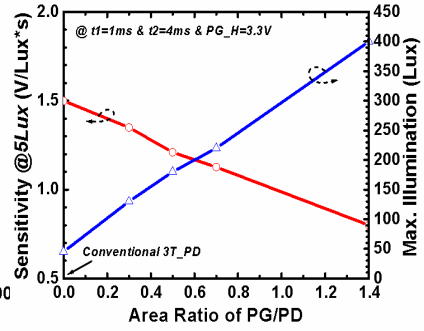


Fig.8. Measured result of sensitivity and maximum detectable illumination with varied PG area.

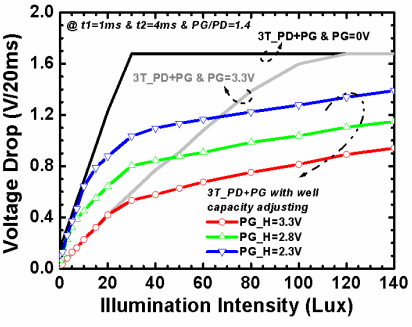


Fig.9. Output characteristics of the proposed pixel with varied PG pulse high levels.

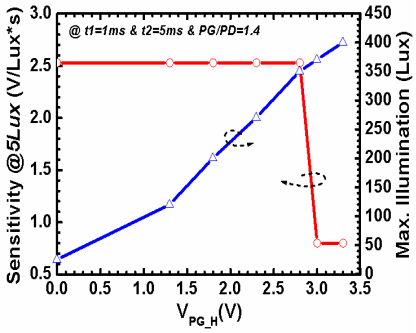


Fig.10. Measured result of sensitivity and maximum detectable illumination with varied PG pulse high levels.

Pixel Type	Original	Novel
Pixel Size	7.5μm x7.5μm	
Operation Voltage	3.3V	
Fill Factor	49%	49%
Dynamic Range	46dB	> 72dB
Sensitivity(V/Lux*s)	1.5	2.5
Dark Signal(mV/s)	421	330

Table I. Pixel performance comparison