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Robust TiN/AHO/HSG-Cylinder Capacitor for High Density DRAMs

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1. Introduction

As DRAM requires high density and high performance, enough cell capacitance is required. The typical method of increasing cell capacitance is to increase the height of storage node (SN). Lots of efforts have been concentrated on the increase of SN height. However, most of them require additional processes [1,2]. The other ways to increase it is to implement high-k dielectrics and/or hemispherical grain (HSG). In this paper, we developed a novel robust capacitor without any additional processes through diagonal cell array scheme and double mold oxide (DMO). Also, we developed a HSG-cylinder Al_2O_3/HfO_2 (AHO) capacitor for the first time in mass production.

2. Process Integration of robust TiN/AHO/HSG-Cylinder Capacitor

Increase of the SN height causes the instability of SN and twin bit fail. The mechanical stability of SN is closely related with the bottom size of SN. The larger bottom size becomes, the higher height of the SN can be obtained [2]. We developed SN in diagonal cell array scheme in order to enlarge the bottom size of SN. In order to accommodate square layout of SN in straight cell array scheme, an additional photo mask is introduced to electrically connect the SN with the SN contact plug [1,2]. But, additional photo mask is not necessary in the case of SN in diagonal cell array scheme. As shown in Fig.1, SN in diagonal cell array scheme, where active areas are tilted, can increase the minimum pitch of SN by approximately 50%, compared to conventional SN in straight cell array scheme [3]. Fig. 2 shows the schematic diagram of active area, SN contact and SN in straight and diagonal cell array schemes.

Multiple mold oxide process makes possible to enlarge the bottom size of SN and to increase the height of SN compared to single mold oxide (SMO) [2]. Additional enlargement in bottom size and the increase of SN height are possible by optimizing the ratio of lower and upper mold oxides. Fig.3 shows the SN cylinder formed with SMO, double mold oxide1 (DMO1) and double mold oxide2 (DMO2). Fig.4 shows DMO1 and DMO2 processes can enlarge the bottom size of SN by 10% and 5% respectively, compared to SMO, and can make increase of SN height by 12% and 6%, respectively. SN in diagonal cell array scheme increases the bottom size and the SN height by 50% and 20% respectively, compared to SN in straight cell array scheme. The cylinder structure with the bottom size of 235nm and the height of 2.0㎛ was achieved by using the DMO in the diagonal cell array of 0.11㎛ technology.

HSG formation is also commercially used to increase capacitance of SN. However, as DRAM size shrinks down, HSG formation is difficult due to decrease of the physical space between the SNs in the cylinder type SN [4]. In this paper, reverse HSG one cylinder storage node (RSOCS), which grows HSG only inner sidewall of cylinder, is developed without decreasing the space between the SNs. Fig. 5 shows the fabrication process flow to make the robust TiN/AHO/HSG-cylinder capacitor with newly developed techniques. First DMO is deposited, and SN lithography and etching process follow. After forming HSG on SN material, cylinder type SN is formed by lift-off process. Finally, AHO dielectric film of 25nm equivalent SiO2 thickness is deposited by ALD method and then TiN is deposited as the top electrode. Fig. 6 shows the top-view and cross-sectional SEM images of the HSG cylinder in diagonal cell array scheme.

3. Characteristics of robust TiN/AHO/HSG-cylinder Capacitor

Cell capacitances are compared with respect to the different schemes of SN in Fig.7. Cell Capacitance of SN in diagonal cell array scheme is improved up to 25% compared to that of SN in straight cell array scheme. Cell capacitances of DMO1 and DMO2 are improved up to 15% and 7% compared to cell capacitance of SMO, respectively. In addition to it, we achieved cell capacitance of 36fF/cell through HSG process, increased by 11%. Fig. 8 shows the cell capacitance and breakdown voltage of SN with respect to the SMO and DMO2 in the straight cell array, and the DMO2 in diagonal cell array. The breakdown voltages are ~2.5V irrespective of the schemes of SN. Fig. 9 shows the capacitance and breakdown voltage of Al_2O_3 (ALO), AHO and HSG-merged-AHO. Cell capacitance of AHO capacitor is improved by 10 % and breakdown voltage is decreased by 3% compared to those of ALO capacitor. Cell

capacitance of HSG-merged-AHO capacitor is improved by 15 % and breakdown voltage is decreased by 2% compared to those of AHO capacitor.

4. Conclusions

Robust TiN/AHO/HSG-cylinder capacitor SN with diagonal cell array scheme and optimized DMO is developed for high density stand-alone and embedded DRAM. Cell capacitance of 36fF/cell and SN height of 2.0㎛ um were obtained in 0.11㎛ DRAM technology. This technology is expected to be extended to sub 0.10㎛ DRAM technology.

References

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[3] S. Kimura et al., IEEE Trans. Electron Devices, vol. 37, no. 3, p. 738 (1990)

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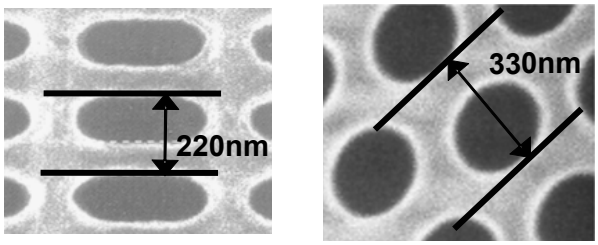
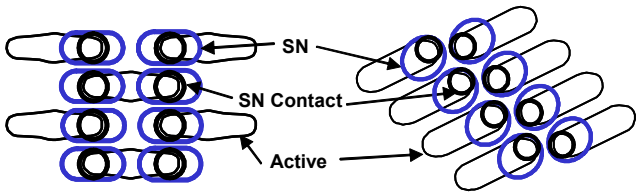


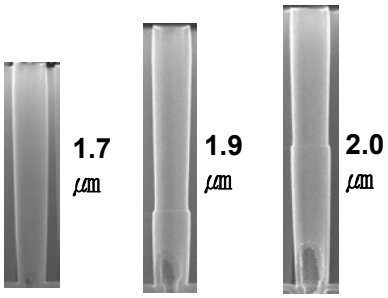
(a) SN in straight cell array (b) SN in diagonal cell array

Fig. 1 Top-view SEM images of SN in straight and diagonal cell array scheme.



(a) SN in straight cell array (b) SN in diagonal cell array

Fig. 2 Schematic diagrams of active area, SN contact and SN in straight and diagonal cell array scheme.



(a) SMO (b) DMO1 (c) DMO2

Fig. 3 Cross-sectional SEM images of SMO, DMO1 and DMO2

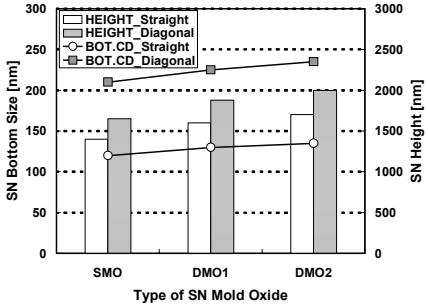


Fig. 4 SN bottom size and SN height with respect to the different SN schemes

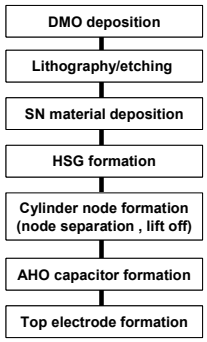
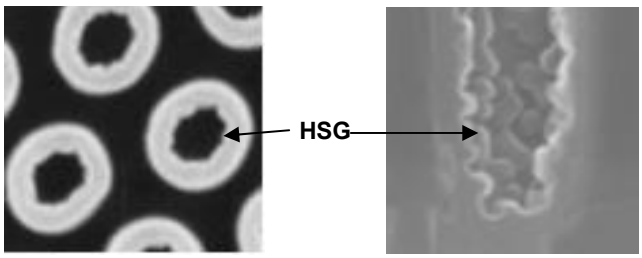


Fig. 5 Fabrication process of robust TiN/AHO/HSG-cylinder capacitor



(a) Top-view SEM images (b) Cross-sectional SEM image

Fig. 6 Top-view and cross-sectional SEM image of HSG-cylinder capacitor.

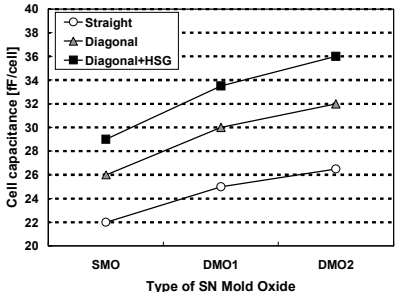
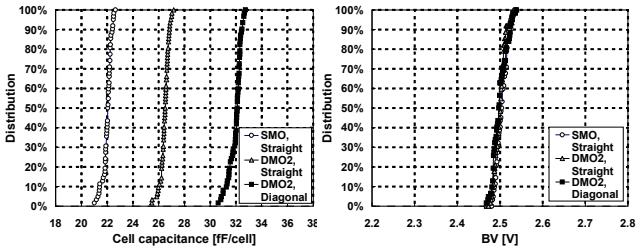
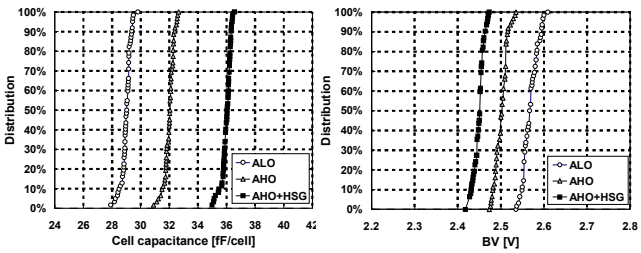


Fig. 7 Cell capacitance with respect to the different SN schemes



(a) Cell capacitance (b) Breakdown voltage

Fig. 8 Cell capacitance and breakdown voltage with respect to SMO, DMO2 in straight cell array scheme and DMO2 in diagonal cell array scheme



(a) Cell capacitance (b) Breakdown voltage

Fig. 9 Cell capacitance and breakdown voltage with respect to ALO, AHO and HSG-merged-AHO