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Effect of Strain on Static and Dynamic NBTI of pMOSFETs

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1. Introduction

Recently, application of mechanical stress in MOSFET channel region has been extensively investigated [1-3]. Various approaches were adopted for enhanced device characteristics and circuit performance. Most of these reports focused on the carrier mobility and drain current improvement, but only few of them addressed about the impact of mechanical stress on device reliability, especially the negative bias temperature instability (NBTI) for scaled CMOS technologies [4].

In this paper, we present the degradation behavior and mechanism of different compressive stress channel pMOSFETs under static and dynamic NBTI. In addition, a threshold voltage (V_{th}) recovery mechanism for dynamic NBTI is proposed in this work.

2. Experimental

The devices in this work were pMOSFETs with 1.6nm nitrided oxide as the gate dielectric. The different compressive stress levels in channel regions are generated by a process strained Si (PSS) technology [5]. The PSS technology comprises individual or multiple process-induced strain methods, for example, STI [1], silicide [2], contact etch stop layer [3] etc., modulating the stress level in three dimensions. The cross-section of strained Si device for HCS and LCS channel pMOSFETs is shown in Fig. 1. By modulating the stress level from PSS technology, pMOSFETs with high compressive stress (HCS) and low compressive stress (LCS) channels were characterized for NBTI.

3. Results and Discussion

Figure 2(a) shows the I-V characteristics. Subthreshold swing and short channel behavior of these two approaches are similar. From high-frequency C-V measurement (Fig. 2(a) inset), the same stretch-out behavior of both curves implies that interface state density is similar in both cases [6]. Figure 2(b) and its inset show the gate leakage and the gate oxide breakdown voltage measured under inversion. Gate leakage and gate oxide breakdown voltage seem to be insensitive to the compressive stress change in the channel.

Static NBTI

Static NBTI is characterized at elevated temperature (T=125, 150℃) and negative gate bias (V_g= -2.4V), and the degradation mechanism is generally attributed to interface traps generated due to Si-H bonds dissociation at Si/SiO_2 interface (interface reaction) and subsequent hydrogen diffusion into gate dielectrics (diffusion reaction) [7]. The dependence of bias temperature induced threshold voltage shift ($\Delta V_{th,BT}$) on channel width and lateral length of active region is shown in Fig. 3. The static $\Delta V_{th,BT}$ difference between these two cases is relatively small and is insensitive to the compressive stress level applied to the channel region.

To characterize the influence of compressive stress on V_{th} degradation, different stressing temperatures were used (Fig. 4). Compared to HCS channel pMOSFETs, the LCS case shows less V_{th} shift under long-term, heavy stressing conditions. Despite these differences, the dependence of $\Delta V_{th,BT}$ on stressing time still approximately follows the power law relation with exponent in the range of 0.2~0.3 (Fig. 4(b)) [7, 8]. This relation implies that the rate of the released hydrogen being consumed through diffusion into the gate oxide may be similar for different compressive stresses [8].

Dynamic NBTI

The dynamic NBTI behaviors of strained channel pMOSFETs are presented in Figs. 5 and 6. Figure 5 shows that the splitting between static and dynamic NBTI is ascribed to V_{th} partial recovery when the negative gate bias (stress phase) is removed and positive gate bias (relax phase) is applied. Such V_{th} recovery behavior persists until stress is resumed. In addition, the NBTI-induced V_{th} shift gradually saturates after several cycles (Fig. 5(b)). Figure 5(b) also shows that the recovered V_{th} amount in relax phases is similar for both cases, although HCS case depicts a more severe V_{th} degradation in stress phases. Thus under dynamic NBTI measurement, the curves of $\Delta V_{th,BT}$ for both cases gradually depart from each other (Fig. 5(a)). Different frequency measurements also demonstrate that LCS case has ~2X lifetime as shown in Fig. 6(a). It is suggested that the different compressive stresses, as compared to HCS case, primarily affect the interface reaction of NBTI mechanism rather than the diffusion reaction [8].

From high-frequency charge pumping measurement, the generated interface traps increase gradually in stress phase and remain stable in relax phase for these two approaches (Fig. 6(b)). It is inferred that the repassivation of Si dangling bonds (i.e., reversible reaction of Si-H dissociation) may be not responsible for the V_{th} recovery. In fact some slower interface traps, i.e., border traps or slow states, can not respond to the high frequency signal. Since oxide traps (e.g., less than 3nm) may be treated as border traps, especially for nitrided oxide, the trapping and detrapping

behaviors of slow states may be responsible for the NBTI recovering mechanism [9]. In addition, HCS channel pMOSFETs may generate more border traps than LCS case and thus results in worse V_{th} degradation after long-term static and dynamic stress.

4. Conclusions

By modulating the stress level using PSS technology, LCS channel pMOSFETs suffers slightly less NBTI V_{th} degradation, compared to HCS case. In addition, trapping and detrapping behaviors of border traps may be responsible for the V_{th} recovery mechanism. Finally, HCS channel pMOSFETs may generate more border traps during NBTI stressing and thus results in worse NBTI degradation after long-term stress.

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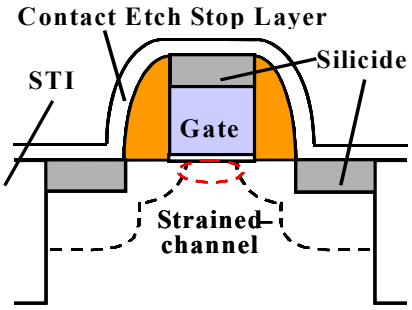

Fig. 1 The cross-section of strained Si device for HCS and LCS channel pMOSFETs.

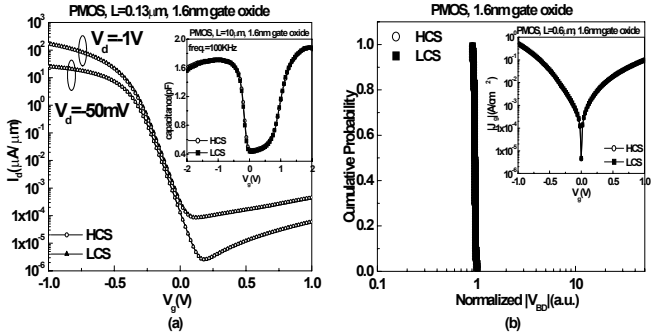

Fig. 2 (a) I-V characteristics (inset: C-V characteristics), (b) normalized gate oxide breakdown voltage (inset: gate leakage), for HCS and LCS channel pMOSFETs.

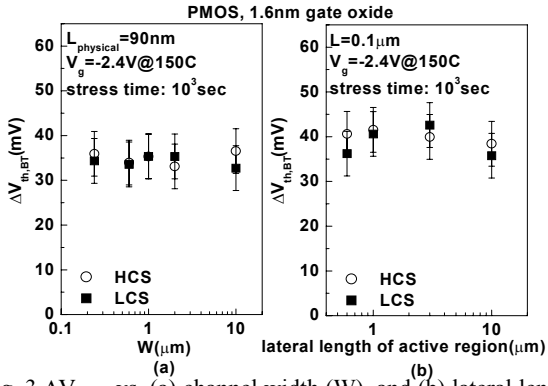

Fig. 3 $\Delta V_{th,BT}$ vs. (a) channel width (W), and (b) lateral length of active region, for HCS and LCS channel pMOSFETs.

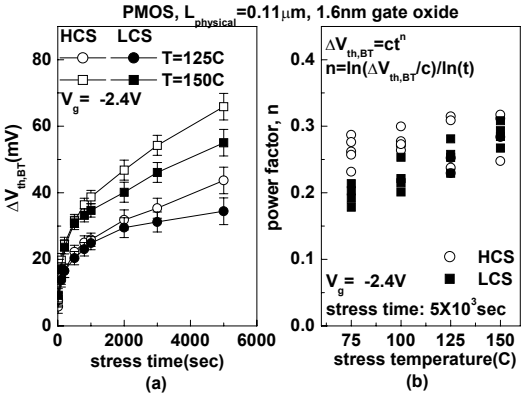

Fig. 4 (a) $\Delta V_{th,BT}$ vs. stress time, (b) power factor (n) at different stress temperatures, for HCS and LCS channel pMOSFETs.

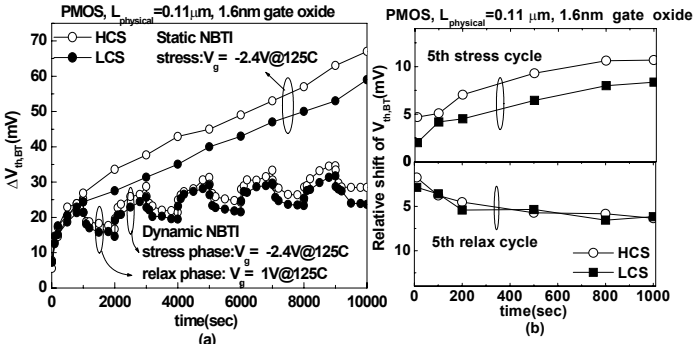

Fig. 5 (a) $\Delta V_{th,BT}$ vs. stress time under static and dynamic NBTI, (b) the relative shift of $V_{th,BT}$ in stress and relax phases for HCS and LCS channel pMOSFETs.

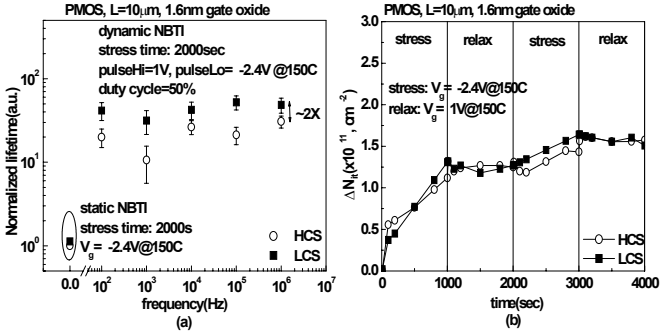

Fig. 6 (a) The frequency dependence on lifetime, (b) interface trap density generated under dynamic stress, for HCS and LCS channel pMOSFETs