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Ge and SiGe for High Performance MOSFETs and Integrated Optical Interconnects

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1. Introduction

It is believed that the difficulty in scaling the conventional Si MOSFET makes it prudent to search for alternative device structures, new material and fabrication technology solutions that are generally compatible with current and forecasted installed Si manufacturing. The saturation of Si MOSFET drain current upon dimension shrinkage limits the prospect of future scaling. Historically it has been believed that as the device dimensions are scaled down the high field carrier velocity saturation diminishes the difference in performance of MOSFETs in different materials. However, it has been recently pointed out that a fundamental scaling limit for MOSFETs is the source injection velocity into the channel limiting the drain current [1]. The lower effective mass (and lower valley degeneracy) of Ge could alleviate the problem by providing a higher source injection velocity [2], which translates into higher drive current and smaller gate delay.

Scaling of VLSI circuits can pose significant problems for interconnects, especially for those responsible for long distance communication on a high performance chip. The near-infrared photodetection and compatibility with Si technology of Ge-based materials, allow simultaneous fabrication of photodetectors and Si CMOS receiver circuits in a monolithically integrated fashion. Such technology could be used for on-chip optical interconnections in global signaling and clocking [3].

Surface passivation for gate dielectric and field isolation and *n*-type dopant incorporation are the two classic problems that obstruct CMOS device realization in Ge. In this paper we present a rview of the rcent activity in this area and application to MOSFETs and photodetectors.

2. High-k dielectrics for Ge passivation

The poor quality Ge native dielectrics for gate insulator and field isolation have been one of the classic problems that obstruct VLSI CMOS device realization in Ge. Efforts to use materials like SiO_2 on a thin Si cap, Ge_3N_4, GeO_xN_y, etc. have been only marginally successful. Inspired by the recent successes of the high-k dielectrics on Si, we investigated the possibility of applying these materials to Ge. Volatility of Ge surface oxides or sub-oxides makes surface cleaning easier for high-k gate dielectric stack free of the performance limiting, lower-k, interfacial GeO_x layer.

We have demonstrated two different techniques to passivate Ge with hi-k dielectrics. In the first technique HfO_2 and ZrO_2 were deposited in a cold-wall high vacuum atomic-layer deposition (ALD) system at 300°C, using alternating surface-saturating reactions of metal tetrachloride and H_2O precursors [4,5]. To study the effect of different surface preparations prior to high-k ALD, gate leakage currents, EOTs and hysteresis from the corresponding MOSCAPs were measured [5]. Among them cyclic rinsing between HF and H_2O (CHF) for cleaning Ge and rapid thermal nitridation (RTN) in NH_3 gave the best results. The optimum dielectric stack (Fig. 1) could be attained by RTN of CHF Ge at 600ºC followed by hi-κ ALD. Excellent C-V curves were obtained from MOSCAPs on both Ge substrate types (Fig. 1) with low leakage. The RTN technique was also employed to passivate the Ge surface prior to the deposition of SiO_2 for field isolation. In the second technique gate dielectric was formed by UHV sputtering of ~22-30 Å Zr films on the Ge surface followed by *in-situ* UV ozone oxidation at room temperature. Ge/ZrO_2 interface was found to be free of any significant interfacial Ge oxide with excellent C-V characteristics with EOT in the range of 6-10 Å [6]. Variants of the high-k on Ge concept have been subsequently demonstrated in Ge MOSFETs by other groups [7,8] showing similar results.

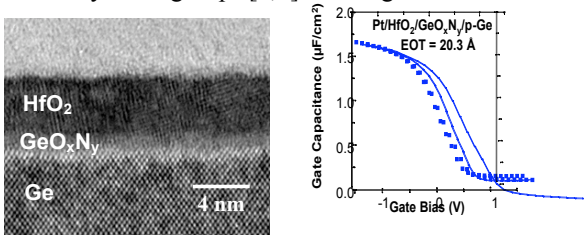

Fig. 1. HRTEM (left) and MOS C-V characteristics (right) of ALD HfO_2 on thin Ge oxynitride (GeO_xN_y) formed by RTN in NH_3 of CHF cleaned Ge surface [5].

3. Dopant Diffusion in Ge

p- and *n*- type dopant incorporation in Ge by was studied [5,6,9] using two techniques: ion implantation and diffusion from doped SiO_2. We demonstrated symmetrically high levels of activation on both *p*- and *n*-type dopants in Ge, at concentrations applicable to advanced CMOS (Fig. 2). The results indicate that ion implanted junctions result in slow *p*-type but fast *n*-type dopant diffusion. To obtain shallow *n*-type profiles solid source diffusion from phosphorus-doped SiO_2 (PSG) was studied as an alternative (Fig. 2).

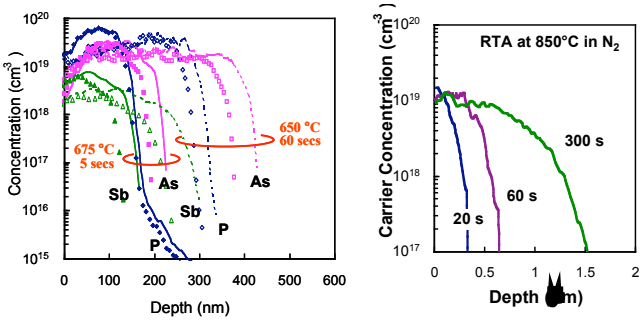

Fig. 2. SRP profiles of various *n*-type dopants in Ge (left) after RTA treatments (675 °C /5 secs and 650 °C/60 secs) [9]. Implantations of various species at a fixed dose of 4×10^{15} cm^{-2} were carried out at energies corresponding to a similar projected range, (right) after 850ºC diffusion from PSG [5].

4. Ge MOSFETs

Using ultrathin ZrO_2 gate dielectric, Ge *p*-MOSFETs were fabricated (Fig. 3) using a low thermal budget (< 400°C)

process [6]. Conventional self-aligned process requires high temperatures for dopant activation, imposing a thermal stability requirement on the high-k gate stack. We demonstrated for the first time Ge *n*-MOSFETs with both HfO_2 and ZrO_2 and metal gates using a simple self-aligned gate-last process. In this process shallow junctions were obtained utilizing dopant diffusion from P-doped oxide [5]. *N*-channel Ge MOSFETs with conventional field isolation were fabricated using a self-aligned gate-last novel process with ALD high-k gate dielectrics and metal gates and optimum source/drain shallow junctions by diffusion from doped oxides [5]. Depletion mode *p*-channel Ge MOSFETs with high mobility have also been demonstrated in Ge nanowires [10].

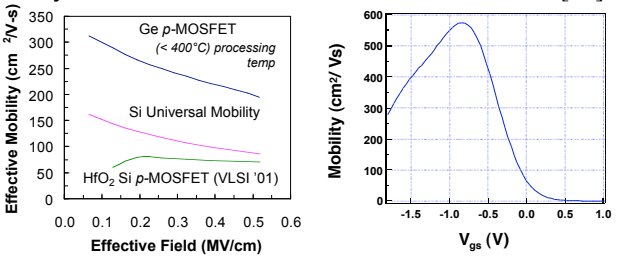

Fig. 3. Mobility of (left) bulk Ge p-MOSFETs [6] and (right) Ge nanowire p-MOSFETs [10] with ZrO_2 gate dielectric

5. Strained Si and Ge Heterostructure Double Gate FETs

In order to enhance performance and continue scaling MOSFETs to the sub-20nm regime, novel, high-mobility materials like strained-Si and Ge (or Si_xGe_{1-x}) are actively being researched for incorporation into the channel. However, due to the aggressive scaling requirements of ultra-thin bodies, high E-fields in the channel and introduction of high-k dielectrics, the channel mobility is severely degraded. We have developed un-doped, Center Channel (CC) NMOS and PMOS FETs (Fig. 4) that incorporate novel transport principles, which fully exploit the advantage of high mobility materials. 1-D Poisson Schrodinger simulations verify that carriers are quantum mechanically confined to a very low E-field region in the center of the DG structure, leading to very high channel mobility. Full-Band Monte Carlo simulations show a ~50% increase in drive currents and ~2X increase in switching speeds at lower capacitance compared to conventional Si DGFETs (Fig. 5) [11]. The cut-off frequencies for the devices are in the terahertz regime, making the device also well suited for analog applications.

6. Ge Optical Detectors

Metal-semiconductor-metal (MSM) photodetectors, are attractive for their high sensitivity-bandwidth product and low capacitance. The near-infrared photodetection and compatibility with Si technology of Ge-based materials, will gallow simultaneous fabrication of photodetectors and CMOS receiver circuits in a monolithic integration fashion. Such technology could be used for on-chip optical interconnections in global signaling or clocking to eliminate many problems associated with large multi-GHz chips like reducing timing skew, power and area for clock distribution. However, relatively large I_{DARK} in Ge photodetectors poses a serious problem. We have demonstrated that application of asymmetric workfunction electrodes can significantly suppress I_{DARK} by tailoring the barrier heights (Fig. 6) [12].

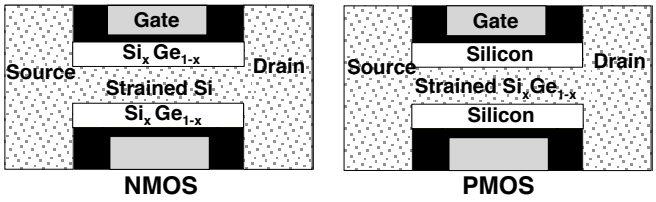

Fig. 4 Device structure and the band diagram illustrating the operation of the heterostructure center channel MOSFETs [11]

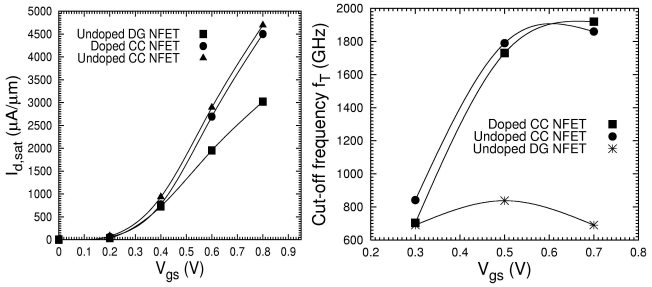

Fig. 5 Simulated drive currents and cut-off frequency for the conventional Si double gate and center channel doped and undoped heterostructure NFETs. [11]

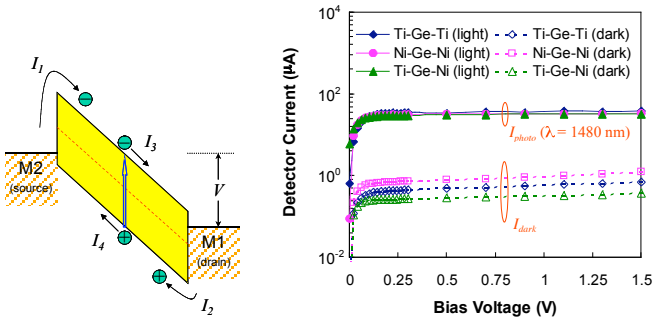

Fig. 6. (Left) Energy band diagram of an asymmetric workfunction MSM photodetector, and (right) experimental photoresponse and dark current of symmetric and asymmetric MSM-photodetectors [12].

7. Conclusions

High mobility MOSFETs have been demonstrated in bulk Ge and in nanowires with high-k gate dielectrics and metal gates. High performance Metal-Ge-metal photodetectors with asymmetric workfunction electrodes to suppress I_{DARK} have been demonstrated.

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