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A Novel STI Process from the View Point of Total Strain Process Design for 45nm Node Devices and Beyond

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1. Abstract

A novel STI process has been proposed for 45nm technologies and beyond. The features of this process are both fluorine-doped SiO2 film for the gap-filling and the following high temperature RTO process for the gate oxidation step. With this technique, the mechanical stress caused by STI is dramatically suppressed.

2. Introduction

Recently, stress-induced mobility enhancement has become one of important technologies, and various types of strains have been introduced in silicon devices [1]. On the other hand, it has been studied that mechanical stress originated from Shallow Trench Isolation (STI) leads to electron mobility degradation depending on transistor layout [2] and increase of junction leakage current caused by band-gap narrowing [3][4] as isolation pitch has been shrunk. Fig. 1 shows the dependence of drain current Id on the distance between channel and STI edge (drain side space Ld = source side space Ls). The Id of NMOS transistor is amazingly degraded as Ld(=Ls) is reduced, while PMOS transistor is less affected. It has been explained that the electron mobility is degraded by compressive stress induced by STI. In order to improve a device performance, it is necessary not only to introduce some new channel strain technique but also to control such a process-induced stress as STI. In this paper, we present the totally strain-controlled STI process using new gap-filling materials and following strain-controlled processes.

3. Experiments

All experimental samples have been prepared through the refined poly-Si buffered mask STI method [5] by which the sacrificial oxidation can be skipped to eliminate influence of other oxidation step except for gate oxide growth. After the liner oxidation step, the F-doped or the conventional SiO2 film was deposited by HDP-CVD using additional NF3 gas or not. F-doped HDP-CVD technique has been reported for narrow gap-filling [6]. To investigate the influences of F atoms, the thermal processes (densification anneal and oxidation for thick gate oxide of 7.5nm) are focused. The conventional low temperature pyrogenic oxidation (LT-pyro.) which is a reaction-limited process and high temperature rapid thermal oxidation (HT-RTO) which is a diffusion-limited process are carried out for the gate oxidation step.

4. Results and discussions

Fig.2. indicates the electron mobility degradation which is investigated using the same transistor pattern as Fig. 1. Id degradation of NMOS is effectively minimized in the case of F-doped HDP with HT-RTO. However, when the low temperature pyrogenic oxidation is used instead of HT-RTO, the improvement of Id degradation remains small. The dependence of Id on Ld(=Ls) is relatively small about PMOS since hole mobility is less affected by compressive stress. Fig. 3 shows the junction leakage current of small pitched n+/p and p+/n diodes at Vr=1.5V. It should be noted that if the F-doped oxide is utilized with HT-RTO for the gate oxidation, both n+/p and p+/n junction leakage currents are remarkably improved compared to LT-pyro.

In order to determine oxidation-induced mechanical stress around STI directly, the convergent beam electron diffraction (CBED) method is adopted. Fig. 4(a) shows TEM image of CBED sample and measurement points are plotted with their numbers on it. The evaluated compressive stress for the conventional HDP sample and the F-doped HDP sample is indicated in Fig. 4(b). It should be noted that the compressive stress can be reduced at every points in the case of F-doped HDP oxide. In particular, the stress close to STI has been remarkably suppressed to compare with that of conventional HDP. Next, FTIR and SIMS measurements are performed to evaluate the role of F atoms. Fig. 5, 7 shows the FTIR spectra of F-doped HDP oxide with thickness of 200nm. As shown in Fig.5, during densification annealing, Si-O peak is slightly sharpened and increases a little. It is found that Si-F peak still remains even if the high temperature annealing at 1100ºC is performed. On the other hand, Fig. 6 depicts fluorine depth profiles of the F-doped oxide after densification anneal at 1100ºC. F atoms of the surface region are diffused out. For these results, out-diffused F atoms during annealing would be originated from surplus interstitial atoms. Therefore, it is concluded that Si-F bonds still remain and keep the oxide film coarse when it is annealed in high temperature. In Fig.7, although Si-F peak completely disappears and Si-O peak significantly increases in the case of LT-pyro, no change of the spectrum can be observed in the case of HT-RTO. It can be explained that under the reaction-limited condition of LT-pyro. process, oxidant can easily diffuse into STI and substitute Si-O bonds for Si-F bonds during gate oxidation step. Furthermore, oxidation reaction occurs in STI/substrate interface by excess oxidant diffused through the oxide film. This reaction causes volume expansion of STI and a large amount of stress is generated. In case of HT-RTO, these problems can be completely avoided because it is diffusion-limited process. As a result, Si-F bonds still remain in filled oxide. From above results, it is considered that the Si-F bonds make gap-filling oxide coarse and reduce STI stress.

5. Conclusions

A totally strain-controlled STI process using the F-doped-HDP-CVD method with the diffusion-limited high temperature oxidation process has been proposed. Employing this method, STI originated mechanical stress is effectively suppressed. Lots of Si-F bonds exist in the F-doped oxide and make gap-filling oxide coarse even after the following processes.

Acknowledgement

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References

[1]T. Ghani et al, IEDM Tech. Dig., pp.978-980, 2003
[2] G. Scott et al., IEDM Tech. Dig., pp.827-830, 1999
[3] P. Smeys et al., IEEE Trans. Electron Devices, Vol.46, pp.1245-1252, 1999
[4] T. Kuroi et al., IEDM Tech. Dig., pp.141-144, 1998
[5] K. Horita et al, Symp. on VLSI Tech. Dig., pp.178-179, 2000
[6] Y.W. Cha et al, Symp. on VLSI Tech. Dig., pp.153-154, 2003

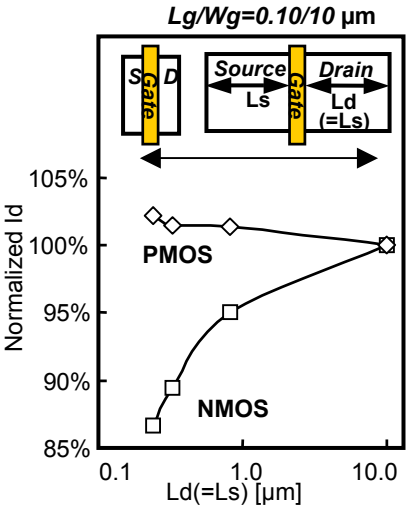


Figure 1 Normalized Id dependent on Ld(=Ls) for the transistors fabricated with conventional processes. Id is normalized to 1 for the Ld=Ls=10μm transistor.

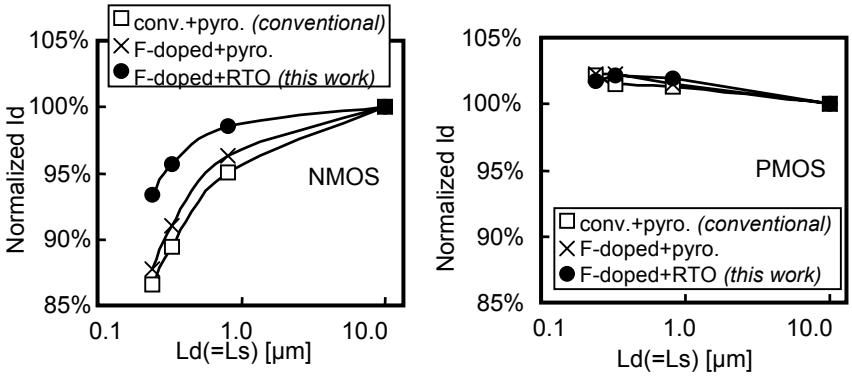


Figure 2 Improvement of the Id degradation of NMOS transistors. F-doped oxide filled STI with HT-RTO process clearly minimizes the NMOS Id degradation.

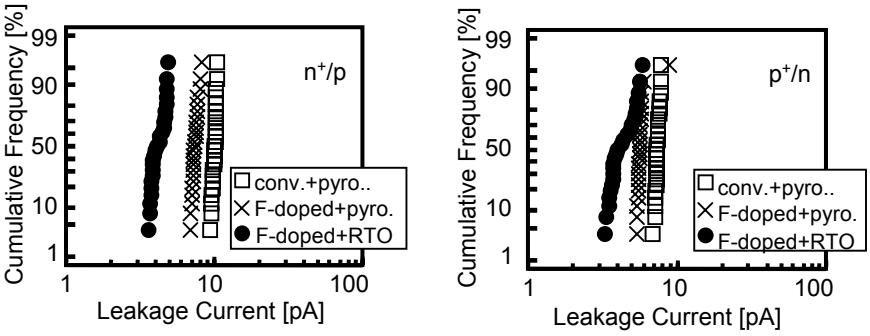
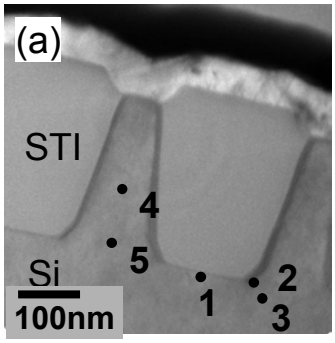


Figure 3 Improvement of the junction leakage current of n+/p and p+/n diodes with small pitch patterned STI at Vr=1.5V, which has been measured after all fabrication steps.



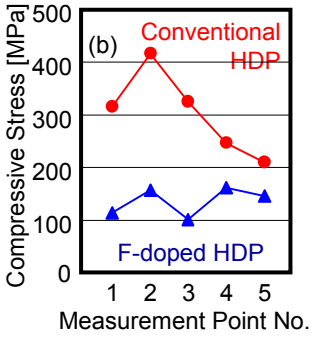


Figure 4 CBED measurement for STI stress analysis.
(a) TEM image with No. of measurement points
(b) evaluated compressive stress

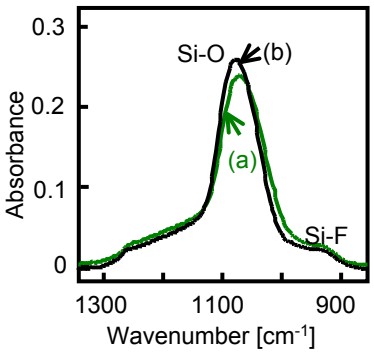


Figure 5 FTIR spectra for F-doped HDP films.
(a) as-deposition
(b) annealed in 1100ºC
Si-F peak around 930cm^{-1} still remains even after high temperature annealing.

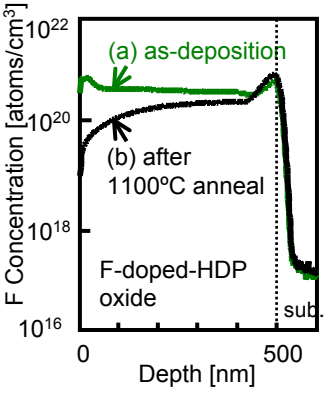


Figure 6 F profiles of F-doped-HDP oxide by SIMS.
(a) as-deposition
(b) annealed in 1100ºC
Interstitial F atoms around surface region are out-diffused.

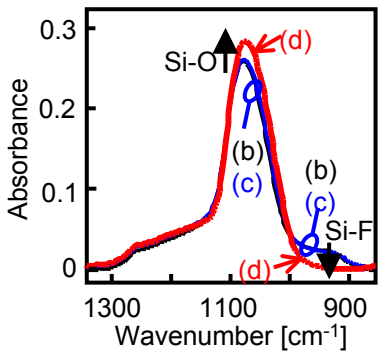


Figure 7 FTIR spectra for F-doped HDP films.
(b) after densification (same as (b)in Fig.5)
(c) HT-RTO performed
(d) LT-pyro. performed
In the case of LT-pyro., Si-F peak disappears and Si-O peak significantly increases.