

B-1-1 (Invited)**Electrical Characterization of High-k Gated MOSFETs and Interfaces**

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Abstract

Some important issues related to the electrical characterization of high-k dielectrics will be reviewed and discussed. The problems with the conventional mobility extraction methodology for high-k gated MOSFETs will be pointed out, and an improved methodology will be demonstrated. Trapping in high-k gate dielectrics can significantly affect electrical measurements, and presents a serious reliability problem. In many samples, the device's operating lifetime may be limited by the trapping-induced threshold shift rather than TDDB. Since some of the trapping events can occur with a very short time constant, pulsed measurements are necessary to capture these events. A novel electrical characterization technique, named the IETS (Inelastic Electron Tunneling Spectroscopy), will be shown to be capable of revealing a wealth of information of a MOS structure, including phonon modes of both the electrodes and the gate dielectric, impurity bonding structures, and electronic traps.

1. Introduction

The 2003 ITRS [1] calls for gate dielectrics of less than 1 nm in equivalent oxide thickness (EOT) in the near future, with a very low gate leakage current. Most experts believe that only some sort of high-k gate dielectrics will be able to fulfill these requirements.

The first group of high-k dielectrics that was proposed to replace SiO₂ consisted of silicon nitride or silicon oxynitride [2,3]. The concept of using a high-k dielectric's larger physical thickness to achieve the same EOT so as to reduce the tunneling leakage current was clearly presented in [2], and the search for the best high-k gate dielectric has continued ever since. This talk will focus on electrical characterization as a tool to help to facilitate high-k materials/process development, and to assess the performance and reliability of resulting devices. Because of the space limitation, only a few examples will be given in this paper.

2. Current Transport in High-k Gate Dielectrics

Since gate leakage is the primary reason for switching to high-k gate dielectrics, we need to understand the current transport mechanisms in high-k gate dielectrics. By

analyzing temperature dependence of the I-V characteristics, one may determine the dominant conduction mechanisms, typically including Schottky emission, Frenkel-Poole conduction, and tunneling, of which tunneling typically dominates at 77K, from which barrier heights and effective mass can be determined by using two different gate electrode [4].

3. Channel Mobility Measurements

It is now well known that the channel mobility in a high-k gated MOSFET is typically much lower than its SiO₂-gated counterpart. Since it is also well known that high-k gated MOSFET tends to have more oxide charge and interface traps than its SiO₂-gated counterpart, it's not surprising that many attribute the degraded channel mobility to Coulomb scattering. Upon more careful examination, however, we found that part of the degradation may arise from the soft optical phonons in the high-k gate dielectric that act as "remote phonon scattering centers", which is consistent with the theory proposed by Fischetti et al [5]. In the course of our study of channel mobility, we found that the conventional methodology used to obtain the channel mobility in high-k gated MOSFET gives rise to very large errors, due to the trapping of carriers. Basically, the use of the conventional split C-V method to extract the carrier concentration in the conduction channel over-estimates that concentration due to trapping of carriers, which results in an underestimate of the channel mobility [6]. This error could be as high as 30-50%, based on the typical interface trap density of high $10^{11}/\text{cm}^2$ to low $10^{12}/\text{cm}^2$ [6]. Therefore, we have introduced a modified split C-V method to more accurately extract the channel mobility [6]. It should be noted that trapping/detrapping time constants for some of the high-k gate dielectrics, including HfO₂ and Al₂O₃, are much shorter than those for SiO₂ [7], and therefore the DC measurement methodology commonly used for MOS devices with SiO₂ gate dielectric will likely to miss these traps. A transient (pulsed) measurement methodology has been introduced to reveal more fully the traps in high-k gate dielectrics [7].

Using the more accurately determined mobility data, we have analyzed the possible scattering mechanisms that may have caused the degraded mobility in high-k gated MOSFETs, and concluded that Coulomb scattering

indeed plays a critical role in reducing the channel mobility in high-k gated MOSFET. In addition, we have also gathered evidence that supports the “remote phonon scattering” theory proposed by Fischetti, et al [5].

3. Reliability

As previously mentioned, charge trapping in high-k gate dielectrics may be a dominant reliability concern for various samples that we have tested. Compared to device-quality SiO₂, the state-of-the-art high-k gate dielectrics based on HfO₂ exhibit significantly higher trapping probability. For many HfO₂-based gate dielectrics that we have tested, the operating lifetime extracted from the trapping-induced threshold voltage shift is much shorter than that extracted from TDDB. Another important feature of trapping events in high-k gate dielectrics is their very short time constants compared to those found in SiO₂. As a result, pulsed measurements are recommended for accurately probing trapping effects in high-k gate dielectrics [7].

5. Inelastic Electron Tunnelling Spectroscopy

This section introduces a novel technique to probe phonons, traps, microscopic bonding structures, and impurities in high-k gate dielectrics with a versatility and sensitivity that are not matched by other techniques. This technique is called the Inelastic Electron Tunneling Spectroscopy (IETS) [8,9], which basically takes the 2nd derivative of the tunneling I-V characteristic of an ultra-thin MOS structure.

The basic principle of the IETS technique is described below. First, without any inelastic interaction, the tunneling I-V characteristic is a smooth curve, and its 2nd derivative is featureless. When the applied voltage causes the Fermi-level separation to be equal to the characteristic interaction energy of an inelastic energy loss event for the tunneling electron, then an additional conduction channel (due to inelastic tunneling) is established, causing the slope of the I-V characteristic to increase at that voltage, and a peak in its 2nd derivative plot, where the voltage location of the peak corresponds to the characteristic energy of the inelastic interaction, and the area under the peak is proportional to the strength of the interaction.

In a typical MOS sample, there are more than one inelastic mode, as a wide variety of inelastic interactions may take place, including interactions with phonons, various bonding vibrations, bonding defects, and impurities. We have obtained numerous IETS spectra of MOS structures with HfO₂ as gate dielectric, and they all show features below 80 meV that correspond to Si phonons and Hf-O phonons, and some features above 120 meV that correspond to Hf-Si-O and Si-O phonons.

Thus these IETS spectra confirm the strong electron-phonon interactions involving optical phonons in HfO₂, and that the Hf-O phonons have very similar energy range as Si phonons which we know are a source of scattering centers that degrade the channel mobility. Therefore, these data indirectly support Fischetti’s “remote phonon scattering model” [5].

IETS can also be used to probe electronic traps in gate dielectrics [9], as electronic traps exhibit identifiable signatures in the IETS spectra. We have found that it’s possible to reveal the spatial locations and energies of these electronic traps by analyzing the IETS spectra in both voltage polarities, and the details of which will be presented at the conference.

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