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1.2nm HfSiON/SiON stacked gate insulators for 65nm-node MISFETs

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Abstract

We realized the Hf-based gate stack with an EOT of 1.2 nm that has a high mobility (N/P:87/96% of that of SiO_2 gate) as well as a low leakage current (a factor of 1/1000). With reducing EOT, the interfacial trap density (D_{it}) increases by the diffusion of Hf atoms through underlayer SiO_2 and degrades the mobility. SiON (N:3%) underlayer is effective to suppress Hf diffusion, which leads the reduction of the D_{it} and high mobility. Nitridation of a HfSiO film is also effective to maintain the leakage current reduction ratio down to the equivalent oxide thickness (EOT) of 1.2 nm. These processes realize high mobility and lower leakage in our 1.2nm-EOT gate stack.

1. Introduction

High-k gate insulator is required for low power device operation. Recently, high–performance, low-power circuit operation was achieved in 90nm node devices by using a HfSiO/SiO_2 (EOT=1.6nm) gate insulator [1,2]. It is difficult, however, to maintain a high I_{on} and a low leakage current with a thinner gate insulator (EOT=1.2nm), which would be required for 65nm node devices. We have thus investigated the reasons for the degradation in leakage current and FET performance caused by the reduction in the gate insulator thickness. In this report, we present a gate insulator structure suitable for 65nm node devices.

2. Experiment

MISFETs with a gate insulator film consisting of HfSiO and HfSiON were fabricated. 2nm-thick of MOCVD HfSiO films were grown on the various thickness of SiO_2 or SiON ([N]=3%) underlayer (thickness of 0.5-2nm). HfSiON films were then formed by NH_3 annealing. 150nm-thick Si gate electrodes were deposited by LPCVD using SiH_4 at 500°C and 620°C. To activate arsenic and boron in gate electrode, source, and drain region, 10 seconds of rapid thermal annealing was performed at 1000°C.

3. Results and Discussion

i) Leakage current

Fig. 1 shows the leakage currents of HfSiO/SiO_2 or HfSiON/SiO_2 MISFETs as a function of EOT varied by reducing the thickness of under layer. As thinning the EOT, the leakage current reduction ratio of HfSiO/SiO_2 against SiO_2 decreases. On the other hand, HfSiON/SiO_2 leakage current reduction ratio is almost 1/1000 against SiO_2 even with thinner gate insulator thickness. Through this experiment, it is also found that the HfSiON/SiO_2 leakage current increases and EOT decreases with increasing nitridation temperature against HfSiO/SiO_2, which physical thickness is as same as HfSiON/SiO_2 (Fig.2).

Fig. 3 shows the leakage current with and without nitridation of the HfSiO film. From TEM observations, we confirmed that the thicknesses of HfSiO and HfSiON were exactly the same. A leakage current density increase and strong temperature dependence were observed for HfSiON. The Poole-Frenkel type of leakage current appeared as a result of the nitridation. From this temperature dependence, it was found that a 140mV electron conduction state was generated by nitridation.

Fig. 4 shows EELS (Electron Energy Loss Spectroscopy) data for HfSiO and HfSiON. The results suggest that a band gap narrowing from 5.4eV to 4.3eV was also caused by nitridation (Fig. 5). From these results, it is found that the leakage current increase in Fig. 2 and 3 is due to the band gap narrowing by nitridation of HfSiO. Still the HfSiON film exhibited a lower leakage current (a factor of 1/1000) at a thinner EOT down to 1.2nm (Fig. 1). This is caused by the increase of dielectric constant of HfSiO film. Nitridation increases the dielectric constant from K=12 to K=20 [3], as high as that of HfO_2, and reduces EOT of HfSiO film as shown in Fig.2. Though nitridation increases the leakage current of HfSiO film, it reduces EOT. As a result, the leakage current reduction ratio is maintained with thin EOT as shown in Fig.1.

ii) FET performance as a function of film structure

The mobilities of NFET with HfSiO/SiO_2 and HfSiON/SiO_2 are compared in fig. 6. The trapped and fixed charge density of HfSiO/SiO_2 and HfSiON/SiO_2 MISFET is suppressed not to affect the mobility degradation [1]. Both HfSiO/SiO_2 and HfSiON/SiO_2 shows high mobility (90% compared to SiO_2) at EOT=1.8nm. Mobility is improved by the nitridation in the region of EOT less than 1.5nm. This is caused by the suppression of Hf atoms segregation, which occurs by crystallization [4]. But the problem still remains that mobility degrades by reducing EOT even with amorphous HfSiON/SiO_2.

Fig. 7 shows the results of the charge pumping current I_{cp} (proportional to interface trap density : D_{it}) of NFET with HfSiON/SiO_2. Increase of D_{it} is observed with reducing the underlayer SiO_2 thickness. This D_{it} increase is presumably due to the Hf diffusion through underlayer SiO_2. Fig. 8 shows the mobility of HfSiON with different thickness of underlayer SiO_2, showing large mobility degradation with reducing the underlayer SiO_2 thickness. Fig. 9 shows NFET mobility of HfSiO/SiO_2 and SiO_2 as a function of D_{it}. It is clearly found that the D_{it} is main limitation factor for the mobility degradation. Fig. 10 shows the D_{it} of SiO_2, HfSiON/SiO_2, and HfSiON/SiON (N:3%) for EOT=1.2nm. It is shown that the D_{it} of NFET with underlayer SiO_2 are higher than D_{it} of SiO_2. In the case of underlayer SiON (N:3%) structure, however, the D_{it} is almost the same level as D_{it} of SiO_2. The underlayer SiON film is thus effective for the suppression of D_{it} generation by preventing the Hf diffusion. Fig. 12 shows that N/PFET mobility of HfSiON/SiON (N:3%) is higher than that of HfSiON/SiO_2. It has been reported that underlayer SiON degrades mobility of NFET [5]. With the low nitrogen concentration SiON(N:3%) underlayer, however, high mobility of N/PFET were achieved. Finally, the HfSiON/SiON MISFET characteristics are confirmed in table 1. Mobility of N/PFET is 87% / 96% at 1MV/cm against SiO_2 gate film, respectively. Good S factor, lower leakage current, low hysteresis were also demonstrated.

Conclusion

By applying a thermal nitridation process, ultra-thin HfSiON gate dielectrics with an EOT of 1.2nm and a gate leakage current reduction ratio on the order of 3 were fabricated and utilized for 65nm CMOS technology. The fabricated devices also exhibited notably high mobility (N/P = 87%/96%), due to the suppression of interface trap generation by the SiON underlayer.

References

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[3] M. Koike et al., IEDM Tech. Dig., p.107, 2003
[4] T. Yamaguchi et al., IEDM Tech. Dig., p.621, 2002
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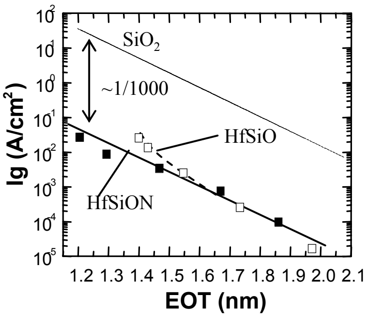

Fig. 1 I_g dependence on EOT of HfSiO and HfSiON

HfSiON maintained an I_g reduction ratio on the order of 3 down to EOT = 1.2 nm.

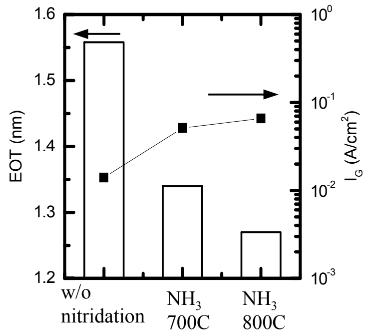

Fig.2 EOT and Ig of HfSiO/SiO$_2$ under various nitridation condition

EOT reduction and Ig increase are observed by nitridation.

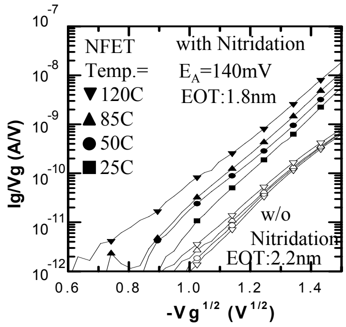

Fig. 3 P-F plot of HfSi/SiO$_2$ and HfSiON/SiO$_2$ leakage current

Through nitridation, leakage current Increases and temperature dependence appears.

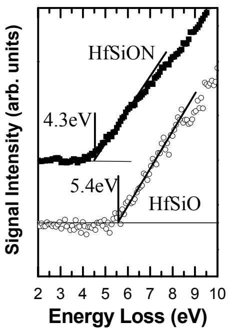

Fig. 4 Band gap measured by EELS spectra

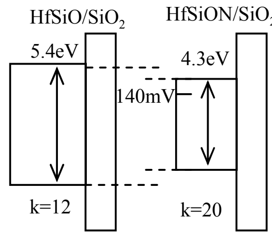

Fig. 5 Band diagram of HfSiO and HfSiON

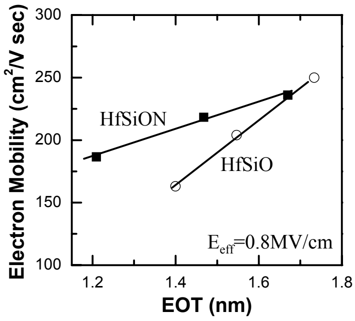

Fig. 6 Mobility dependence on HfSiO and HfSiON

Though nitridation improves the mobility, mobility of HfSiON also degredes by reducing EOT.

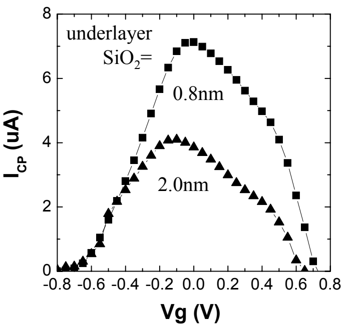

Fig. 7 Charge Pumping Current of HfSiON with various thickness of interfacial SiO$_2$ layer

D_{it} increases with reduction of SiO$_2$ underlayer thickness.

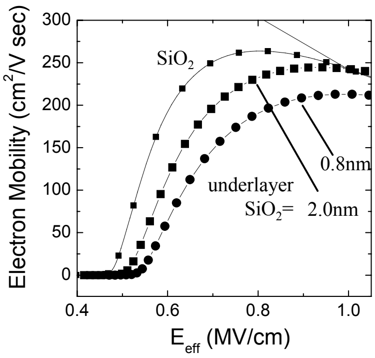

Fig. 8 Mobility dependence on interfacial SiO$_2$ thickness

Mobility also degrades by reducing SiO$_2$ underlayer thickness.

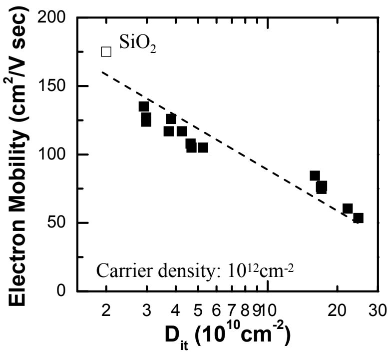

Fig. 9 Relation between mobility and D_{it} in HfSiON/SiO$_2$ NFET at low E_{eff}

Mobility at carrier density=10^{12}cm^{-2} (E_{eff} is around 0.65MV/cm) is shown.

D_{it} reduction is effective to improve mobility.

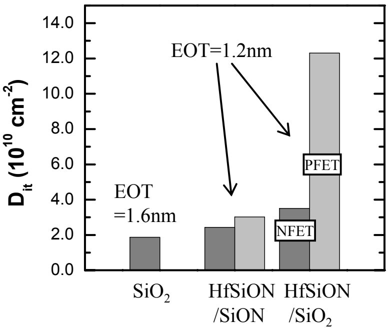

Fig. 10 Interfacial state density of HfSiON with SiO$_2$ or SiON interfacial layer

SiON underlayer decreases D_{it}, especially in PFET.

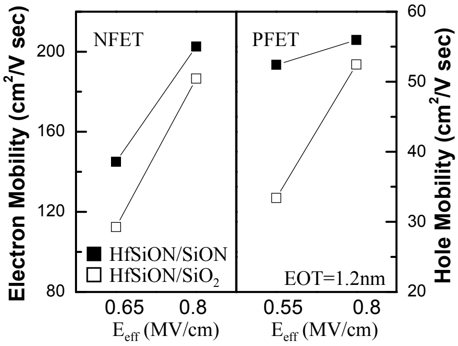

Fig. 11 Mobility of HfSiON with SiO$_2$ or SiON underlayer

3%-SiON underlayer improves the mobility of both NFET and PFET.

Table 1 FET characteristics of our HfSiON/SiON stack

	HfSiON/SiON	
	NMOS	PMOS
EOT (nm)	1.2	
Ig (A/cm^2)	3.2E-02	2.3E-03
Mobility@1MV/cm	87%	96%
S (mv/dec)	72	75
Dit (cm^{-2})	2.3E+10	2.7E+10
Vth Shift (V)	0.11	-0.59
Hysteresis (mV)	0.3	-0.3