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Scaling of Multiple-Gate Fully Depleted SOI Transistors

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1. Introduction

The purpose of this work was to model non planar multiple gate FD-SOI structures over a large, multidimensional space of the critical process parameters. The primary goal was to characterize this large domain, and to locate the critical operating points. A secondary goal was to analyze this domain for the important relationships between the process parameters and the electrical responses, in order to evaluate the performance versus Fin dimensions and the scaling rules of such transistors.

2. TCAD setup

The approach taken in this work was to combine a DOE/RSM method with 3D TCAD (Technology CAD), using commercially available software for both. The DOE (Design of Experiments) feature reduces the number of TCAD runs that are required to characterize a large-dimensional process space. An empirical RSM (Response Surface Model) model is then generated for the TCAD results. This RSM model of the TCAD results enables Target values to be located within the entire domain, and provides ready visualization of the responses in 2D or 3D Contour Plots.

The goal of this work was to analyze the 3D TCAD results for a non planar FD-SOI structure with Polysilicon gate for 65 and 45 nm nodes, i.e. at short Lg of 20-30 nm. The key process parameters were included in the TCAD. A p-type body doping was fixed to $6e^{18}$ atoms/cm^3 in order to achieve V_T values compatible with CMOS technologies.

Parameter	Domain Range	# Levels
L_G_nm	50 - 20	4
W(Fin)/L_G	0.2 - 3	4
t(SOI)/L_G	0.2 - 3	4
t(BOX)_nm	100	1

Table 1: TCAD domain parameters, ranges and levels.

The gate oxide thickness was fixed to 1 nm, and the supply voltage to 1V. No thick top oxide was assumed on top of the silicon Finger: the transistors have three conduction channels. Abrupt Source/Drain junctions have been assumed in this analysis, with a doping level of $2e^{20}$atoms/cm^3. Classical drift diffusion model was used for the simulation. Table 1 summarizes the 3D process space investigated. The Finger width (W_{FIN}) and the SOI thickness (T_{SOI}) have been normalized to the gate length. The minimum and maximum values for these ratios have been chosen based on simple asumptions. For $W_{FIN}/L_G = 0.2$ and $T_{SOI}/L_G = 3$, we have a FinFET electrical behavior, (i.e. $T_{SOI} > L_G > W_{FIN}$). When $W_{FIN}/L_G = 3$ and $T_{SOI}/L_G = 0.2$, the structure is close to a single gate Fully depleted SOI (i.e. $T_{SOI} < L_G < W_{FIN}$). Between those two extreme conditions, we have the triple gate transistor, for which $W_{FIN}/L_G \sim 1$ and $T_{SOI}/L_G \sim 1$ (i.e. $T_{SOI} \sim L_G \sim W_{FIN}$).

3. TCAD results and discussion

The output variables extracted from the simulation are the subthreshold slope (SS), the DIBL, the leakage (I_{OFF}) and saturation (I_{ON}) currents. As the subthreshold slope is one of the most sensitive parameters for the control of short channel effects, we decided to optimize SS in order to improve and to have a good control of the short channel effects.

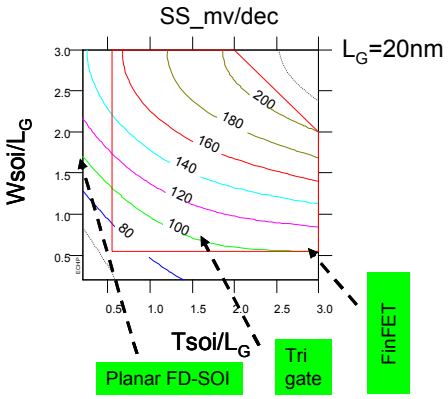

Figure 1: Iso subthreshold slope values versus Finger width and SOI thickness for a 20nm gate length transistor

Fig.1 shows the Contour Plot representation of the empirical models generated in the Domain, for SS in the case of a 20nm effective gate length transistor. Iso SS values are plotted versus T_{SOI} and W_{FIN}. Multiple SOI thickness and Finger width combinations can satisfy the 100mV/decade condition for SS. A wide and ultra-thin SOI layer (i.e. planar Fully Depleted SOI transistor) achieves the same SS as a triple gate (Tri-gate) transistor (narrow and thin SOI layer) and as a dual-gate FinFET transistor (very narrow and thick SOI layer). This representation is very efficient for visualizing the entire domain of non planar SOI transistor designs. For a given gate length, it becomes easy to de-

termine T_{SOI} and W_{FIN} that satisfy a given SS condition. Scaling rules (i.e. Fin dimensions leading to the targetted SS value) can thus be defined.

Figure 2 represents the iso subthreshold slope curves as a function of the gate length and the ratio of the SOI thickness to the gate length.

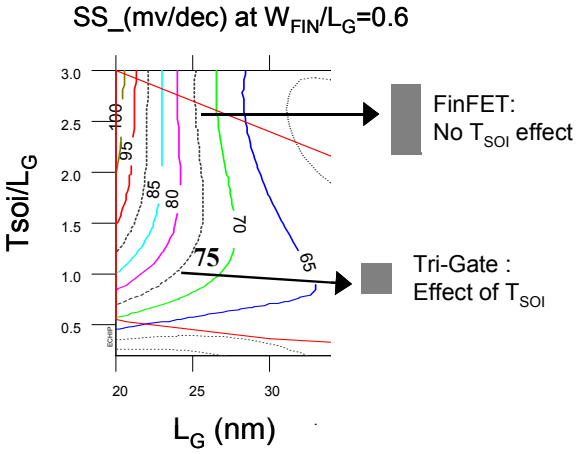

Figure 2: Iso subthreshold slope values versus T_{SOI} to gate length ratio and effective gate length. The Finger width to gate length ratio is fixed to 0.6 in this Figure..

It shows that for a gate length of 25 nm and W_{FIN}/L_G=0.6, a subthreshold slope of 75mV/decade is achieved for T_{SOI}/L_G=1.5. Above 1.5 (i.e. thicker T_{SOI}), the SS value stays constant (i.e. is independent of T_{SOI}). This corresponds to a FinFET case and W_{FIN}/L_G can be tuned to get the targetted SS value. Below 1.5, the reduction of T_{SOI}/L_G ratio improves the SS value down to 70mV/decade. In this case, both T_{SOI} and W_{FIN} improve the SS value: this is the case of a Tri-gate transistor. By assuming $W_{FIN}=T_{SOI}$ for Tri-gate, the two parameters can be optimized to achieve the SS value.

For those two previous device architecture, the Fin dimensions have been extracted from the contour plots, and the targetted SS value has been fixed to 75mV/decade. Required Finger width (W_{FIN}) and SOI thicknesses (T_{SOI}) are presented versus gate length in Fig. 3 and 4 respectively. W_{FIN} is narrower in the case of FinFET transistors, which was expected, but makes the FinFET more difficult to scale. Compared to previous results [1], we found (Fig. 3) that the Tri-gate transistor requires tighter Finger dimensions for the 20nm effective gate length ($W_{FIN}/L_G=T_{SOI}/L_G$~0.7), whereas the ratios are closer to 1 for 30nm gate length. The dashed area of Fig. 4 represents the allowed T_{SOI} thickness values for the FinFET transistor. In such a device, thicker T_{SOI} provides higher drive current. Trade off between performance and processing issue has to be made. In addition, Fig.4 shows the required T_{SOI} for Single gate Fully Depleted transistors for which T_{SOI}/L_G~0.25. This is based on previous 2D TCAD, and shows that required ultra-thin SOI film thicknesses make the scaling of planar FDSOI transistors very difficult. It is important to note that we can define the Fin dimension for a different SS value, by using the same methodology and the same RSM model. There is no need to run new set of 3D TCAD simulations; the RSM model of the TCAD data provides this extended capability. A more aggressive SS value (i.e. <75mV/decade) will induce tighter dimensions for the Fin. Reversely, a larger value for SS will lead to bigger Fin dimensions.

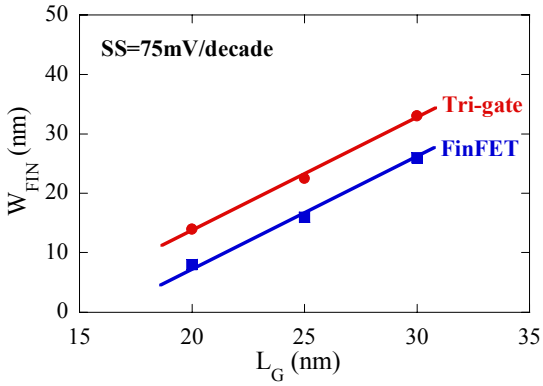

Figure 3: Required Fin width for FinFET and Tri-gate transistors.

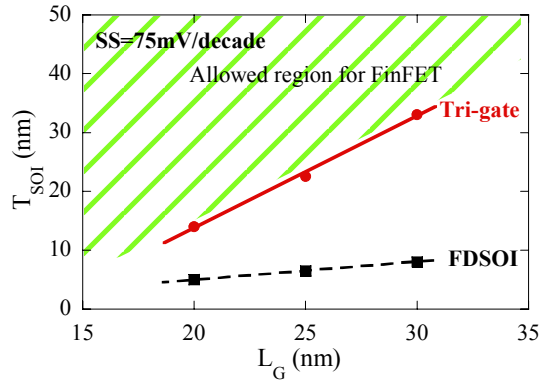

Figure 4: Required SOI thickness for FinFET and Tri-gate transistors. SOI thickness for FDSOI is added for comparison.

3. Conclusions

By using RSM coupled with TCAD, we have developed a methodology for the definition of the scaling rules of FinFET and Trigate transistors. As Lg scales to 20 nm, Trigate will continue to scale further than FinFET due to the inherently wider fin. The apparent T_{SOI} range of FinFETs is not an advantage; it just shows that low SS values can be obtained with high-aspect ratio fins which tend to become non-manufacturable.

References

[1] R. Chau et al, Ext. Abstr. SSDM'02, p.68, 2002.