Device Design Consideration for Four-terminal Double-gate MOSFET (4T-DGFET)

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1. Introduction

In recent VLSI circuits, the power consumption issue becomes very important in addition to the scaling issue. Among many emerging devices, a double-gate MOSFET (DGFET) [1] has widely been recognized as the most scalable FETs due to its high SCE immunity. Furthermore, the DGFET can offer the other advantage of a flexible Vth controllability by evolving the conventional 3-terminal to 4-terminal (4T) DGFTs (Fig. 1) [2-4]. The 4T-DGFET therefore has high potential to achieve evolving VLSI circuits, namely, hot and cool (high performance and low power) circuits. The authors recently succeeded in fabricating the 4T-DGFET by utilizing the advanced FinFET technology, and experimentally demonstrated the highly flexible Vth control [5]. The electrical properties of the 4T-DGFET are dependent on given device parameters, e.g., gate insulator thickness and work functions and on operation condition. 

In this study, the requirements for the 4T-DGFET to realize novel hot-and-cool chips utilizing the unique characteristic of the Vth controllability of the 4T-DGFET is investigated using device simulation [6].

2. Guideline for 4T-DGFET Device Design

We examined an n-channel 4T-DGFET in this work (Fig. 2). Typical Vth curves for the 4T-DGFET are shown in Fig. 3. In this case, G1 was used as a drive gate and G2 as a control gate (single-gate (SG)-mode). Although the s-slope is worse than that in the double-gate (DG)-mode, Vth(G1) in the SG-mode can successfully be controlled by changing Vg2 (Fig. 3(a)). By controlling the Vth(G1), a set of Ioff and Ith can range from a ‘cool’ state to a ‘hot’ state as shown in Fig. 3(b). In this work, Vth in the cool state (Vth(cool)) is set at 10–11 A/μm. In the hot state (Vth(hot)) is set as Ioff when Ith is at 10–7 A/μm. The power supply voltage Vdd is set at 1 V. Ith in the SG-mode for the 4T-DGFET is dependent on the Vth in the DG-mode (VthDG), Vg2 and γ [7–9]. As one can see in Fig. 3(a), VthDG meets Vdd just at Vg2 = Vdd–IthDG. In this state, both the G1 and G2 side channel surface potentials reach the threshold. When Vg2 < Vdd–IthDG, G2 side surface is depleted. In this state, VthDG is expressed as

VthDG = Vdd−(γ(Vdd−VthDG))

(1)

And the s-slope, S, is given by [9]

S = 0.061(1+γ) [mV/dec.]

(3)

If Vdd is defined as Vth at Ioff = 10–7 A/μm, Ith is given by

log(Ith) = (–7–log(W/L)+VthDG)/S

(–7–log(W/L)+VthDG)/S

(4)

Note that VthDG is determined by the DG workfunction φth (VthDG ~ φth~T(10)) and is independent of Tm2.

3. Results and Discussion

The impact of φth on Ioff–Ith characteristics is shown in Fig. 4. Here φth is defined as the workfunction difference between the gate material and n–Si. Obviously, Ioff–Ith characteristics is improved with decreasing φth. This can be understood from the dependence of VthDG and s-slope on Vg2 (Fig. 5). As mentioned before, VthDG meets Vg2 just at VthDG. While Vg2 is less than VthDG, the s-slope is higher than VthDG (22 surface depletion), the s-slope keeps low. After Vg2 exceeds VthDG, i.e., VthDG is higher than VthDG, the s-slope is deteriorated. This is because, once Vg2 exceeds VthDG, the G2 side surface can be inverted (see Fig. 8(a)). Thus, VthDG can be lowered down to VthDG while maintaining low s-slope. A lowering φth, i.e., lowering VthDG apparently extends the useful range of VthDG. As a result, Ioff–Ith characteristics are improved as φth decreases. Note that, a variable range of a set of Ioff and Ith adjusted by Vg2 ≤ |1V| shifts upward with lowering φth. This is due to a negative VthDG shift by lowering φth.

It is apparent from Fig. 6 that increasing Tm2 makes Ioff–Ith characteristics better. Figure 7 shows the dependence of the VthDG and s-slope on Vg2. At Vg2 < VthDG (G2 surface depletion), the s-slope is lower with increasing Tm2, as predicted from Eq. (2) and (3). In addition, the s-slope for thick Tm2 case keeps relatively low even after Vg2 exceeds VthDG. This is because the controllability of G2 becomes lower due to the thick Tm2 and the channel potential is mainly governed by Vg1 (Fig. 8(b)). Thus, increasing Tm2 reduces the s-slope for any Vg2 condition and contributes to Ioff–Ith characteristics improvement. However, a variable range of a set of Ioff and Ith adjusted by VthDG ≤ |1V| is significantly narrower with increasing Tm2 as shown in Fig. 6.

Although Ith(hot) is enhanced by scaling Lth for all Tm2 cases, less advantage of increasing Tm2 is observed in Fig. 9. The variable range of a set of Ioff and Ith adjusted by VthDG ≤ |1V| becomes further narrower and shifts to upper direction for thick Tm2 case. These originate in a significant VthDG roll-off, increase in s-slope and decrease in γ for thick Tm2 4T-DGFET with scaling Lth as shown in Fig. 10. The decrease in γ is explained by a reduction in G2-channel capacitance due to an increase in drain-channel capacitance [11]. It should be noted that all SCEs, i.e., VthDG roll-off, degradation of s-slope and γ can be suppressed by decreasing Tm2.

It is obvious form Fig. 9 that, at φth = 0 eV, Lth cannot reach Lth(cool) under the condition where VthDG is limited to |1V|, i.e., |1V|. So increasing φth is inevitable to achieve Lth(cool). On the other hand, lowering φth improves Ith–Ith characteristics as shown in Fig. 4. Then we analytically and simulationally estimated the minimum φth necessary for attaining Lth(cool) when Vg2 range is limited to |1V| and then Ith(cool) for the 4T-DGFET having the estimated φth DG. As shown in Fig. 11(a), for Lth = 78 nm case, φth calculated from Eq. (4) agrees with that obtained from a simulation for all Tm2 cases. Although the minimum φth increases by setting a limit on Vg2 range, Ith(cool) is enhanced with increasing Tm2. For Lth = 18 nm case, however, φth obtained from a simulation becomes significantly higher with increasing Tm2 than analytically estimated one (Fig. 11(b)). This is due to a pronounced deterioration of the SCE of the s-slope, γ and VthDG for thicker Tm2 case, as shown in Fig. 10. As a result, when Vg2 range is limited to |1V|, Ith(cool) for 4T-DGFET with the thinnest Tm2 shows the highest value. In conclusion, in the short Lth regime, high VthDG controllability and high SCE immunity for the symmetric Tm2 4T-DGFET can offset the large s-slope issue.

4. Summary

The device design for the scaled flexible Vth DG-DGFET has been examined in terms of Tm2 and φth. Simulation results show that the 4T-DGFET with a symmetric Tm2 (Tm1 = Tm2) and an ultrathin Tm2 is promising for future hot-and-cool chips.

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become severer with increasing reduced and s-slope increases. Note that all the SCEs become lower, \( L_{\text{eff}} \) is scaled down, \( I_{\text{off}} \) is improved. For thick curves, the s-slope is improved with increasing \( L_{\text{DG}} \), i.e., \( V_g \) is lowered, \( I_{\text{off}} \) becomes lower, \( L_{\text{eff}} \) becomes higher, and the variable range of a set of \( I_{\text{on}} \) and \( I_{\text{off}} \) becomes lower with increasing \( T_{\text{mox}} \).

Fig. 4: Dependence of \( L_{\text{on}}, I_{\text{on}} \) characteristics for 4T-DGFET on \( \phi_m \) of the DG material. As the \( \phi_m \) becomes lower, \( L_{\text{on}} \) characteristics are improved.

Fig. 5: Dependence of \( V_{\text{thDG}} \) and s-slope on \( V_g \) for 4T-DGFETs with \( \phi_m=0 \) eV and 0.4 eV. For both cases, \( V_{\text{mox}} \) can be lowered down to \( V_{\text{thDG}} \), while maintaining an acceptable s-slope.

Fig. 6: Dependence of \( L_{\text{on}}/I_{\text{on}} \) characteristics for 18-nm-4T-DGFET on \( T_{\text{mox}} \). As the \( T_{\text{mox}} \) becomes thicker, \( I_{\text{on}}/I_{\text{off}} \) characteristics are improved. The controllability of a set of \( I_{\text{on}} \) and \( I_{\text{off}} \) becomes lower with increasing \( T_{\text{mox}} \).

Fig. 7: \( T_{\text{mox}} \) dependence of \( V_{\text{thDG}} \), \( V_g \) and s-slope for 4T-DGFET. The s-slope is improved with increasing \( T_{\text{mox}} \).

Note that, for thick \( T_{\text{mox}} \) case, s-slope keeps low, even after \( V_{\text{thDG}} < V_g \), i.e., \( V_g \) is higher than \( V_{\text{thDG}} \).

Fig. 8: 2D electron concentration in the channel for 4T-DGFET at \( V_g = -0.5 \) V (\( V_{\text{mox}} \)) and \( V_g = -0.1 \) V (\( V_{\text{thDG}} \)). For thick \( T_{\text{mox}} \) case, G2 side surface is not inverted even when \( V_g \) higher than \( V_{\text{thDG}} \) is applied.