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# Planar Double Gate CMOS transistors with 40nm metal gate for multipurpose applications

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## Introduction

Multi-gates devices [1] represent the most promising architectures to fulfill the roadmap targets for sub-32nm nodes [2]. Among them, planar Double Gate MOS transistors (DG MOS) offer an ability to naturally integrate strained Si required to enhance the transport properties of ultra-scaled devices [3]. Moreover, with independent biasable gates, their properties are usefully tuned. They are thus versatile and evolutionary devices. For the first time, we report a simple process for 40nm planar DG MOS with direct TiN metal gate with tunable threshold voltage. DG MOS are naturally co-integrated with Single Gate Fully Depleted MOS transistors (FD MOS). Channels as thin as 8nm are obtained without any out-of-gate silicon consumption. Excellent performance is reached in double gate operation for 40nm drawn gate length: $I_{on}$=765µA/µm - $I_{off}$=0.42µA/µm for PMOS and $I_{on}$=935µA/µm - $I_{off}$=97nA/µm for NMOS transistors. Both N and PMOS exhibit an excellent control of the subthreshold slope (<67mV/dec) and DIBL (<40mV/V). In addition, as the two gates were designed to allow independent biasing, their threshold voltage can be tuned so that each device can operate between Low-power and High-performance modes.

## Process description

Boron doped ($1.10^{15}cm^{-3}$) (100) SOI wafers served as the starting material (fig.1). The silicon film was thinned down by thermal oxidations. The final channel thickness was around 10nm. After LOCOS isolation, the 2nm thick gate oxide was thermally grown before CVD deposition of the TiN ($TiCl_4$ + $NH_3$) metal gate and in situ doped polysilicon. Ebeam lithography was used to pattern gates with lengths down to 40nm. Thanks to an original dry and wet etching of the poly-TiN gate stack, we can reach very low dimensions without any out-of-gate silicon consumption (fig.2). Molecular bonding on a handling oxidized substrate was achieved. We removed the initial silicon substrate, the buried oxide (BOX) serving as an etch stopper. Then, we patterned front gate (FG) (fig.3) with an alignment on the same ebeam marks as the ones used for back gate (BG) lithography. Front and back gate positions are thus precise enough to allow the realization of specific test structures dedicated to the study of misalignment between FG and BG. This misalignment influence on $I_{on}$ was experimentally measured and found to be in good agreement with simulations (fig.4) and previous studies [5]. The unavoidable misalignment of the DUV patterns induced by bonding does not impact upon the electrical performance determined by ebeam alignment. After extension implantation and spacer formation, Si raised source and drain were selectively grown before nickel salicidation. As shown in figure 5, NiSi (9Ω/□) extends under the nitride spacers to decrease the access resistance [6].The back end sequence follows a standard CMOS process. The final DG MOS is represented on figure 6.

## Electrical results

*Gate stack characterization*

With undoped thin film transistors, work-function ($\Phi_m$) engineering is crucial to adjust the threshold voltage ($V_{th}$). TiN gated capacitors have been fabricated to study the evolution of $\Phi_m$(TiN) as a function of temperature to reproduce the anneals a direct gate is submitted to during the process (fig. 7). Capacitive behavior is kept up to 1050°C and $\Phi_m$ stabilizes around 4.4eV. $V_{th}$ comparison of N and P DG MOS with FD MOS enables us to extract $\Phi_m$(FG) = 4.5eV and $\Phi_m$(BG) = 4.8eV. FG was only subjected to dopant anneal at 1050°C and its $\Phi_m$ is in good agreement with the one extracted for MOS capacitors at this temperature whereas BG was also submitted to bonding anneal and FG stack deposition thermal budget, these additional anneals increased its $\Phi_m$. Mobility extraction was performed on 100nm DG PMOS with oversized BG to get rid of possible misalignment. Mobility was extracted drawing the linear curve $[d^2(1/I_d)/dV_g^2]^{-1/3}$ versus $V_g$ [7]. Results show that the BG mobility is systematically higher than the TG one (fig.8). Chlorine concentration keeps on increasing at the TiN/$SiO_2$ interface during the process (fig.9) and, for the final device, its concentration is even twice at the BG interface compared to the one at the FG interface (fig.10), it indicates that the use of $TiCl_4$ as precursor is not a major drawback for future TiN metal gate integration in PMOS transistors.

*Static performance*

As shown in figures 11 and 12, very good performance is obtained on 40nm drawn gate length DG MOS (80nm physical gate length): $I_{on}$=935µA/µm @ $V_g$-$V_{th}$=1V and $I_{off}$=97nA/µm @ $V_g$-$V_{th}$=-0.2V for NMOS transistors. On the Low Power PMOS characteristics with front and back gates of the same length, $I_{on}$=605µA/µm @ $V_g$=1.2V and $I_{off}$=7nA/µm @ $V_g$=0V. When the BG is oversized compared to the FG, the access resistance to the back channel is decreased and $I_{on}$ increases to 765µA/µm for $I_{off}$=0.42µA/µm for PMOS. As expected, DG MOS exhibit an excellent control of the subthreshold slope (<67mV/dec) and DIBL (<40mV/V) which is quite better than the single gate devices with respectively a subthreshold slope of 80mV/dec and 120mV/dec and a DIBL of 160mV/V and 220mV for NMOS and PMOS.

*Double gate versatility*

On our double gate devices, front and back gates can be biased separately. Thus, they can be used as FD MOS with a tunable $V_{th}$ ranging from Low-stand-by-power (LSTP) or Low-operating-power (LOP) to High-performance (HP) values by modifying the back gate voltage ($V_{bg}$) (fig. 13). They can also be used as tunable threshold voltage DG MOS by applying a bias offset between the two gates ($V_{bg}$-$V_{fg}$). This offers a unique opportunity to integrate multiple $V_{th}$ in future System-On-Chip by using only one device architecture, as evidenced from the $I_{off}$ vs $I_{on}$ curves (fig.14).

## Conclusion

Thanks to bonding and direct metal gates without any out-of-gate Si consumption, High-performance DG MOS with TiN metal gate have been processed. They exhibit excellent control of short channel effects down to 40nm gate length. Moreover, their electrical properties can be tuned between LSTP and HP by independent biasing of the two gates.

## Acknowledgements

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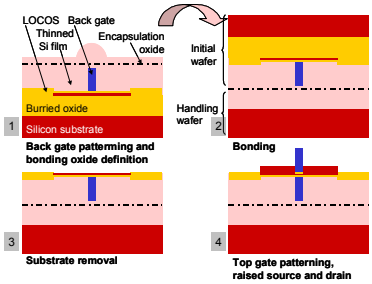


*Fig.1: Process description up to raised source and drain.*

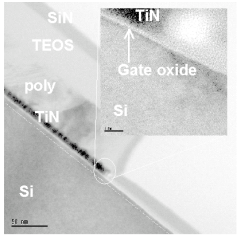


*Fig.2: TEM after gate etching: no out-of-gate Si consumption. Insert : zoom at gate edge.*

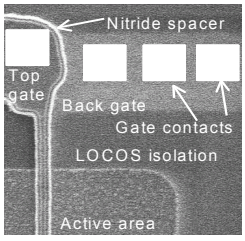


*Fig.3: SEM top view. FG and BG contacts are DUV printed on the ebeam gates (above and below active area).*

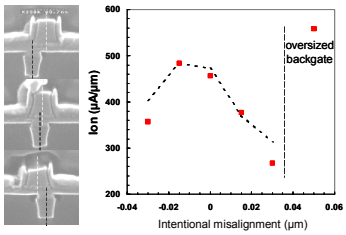


*Fig.4: Left -Misalignment test structures. Right -$I_{on}$ as a function of intentional misalignment for a 50nm DG MOS (points: experiment, dashed line: simulation).*

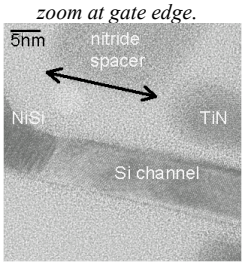


*Fig.5: TEM of NiSi penetration under the spacer and crystalline extension.*

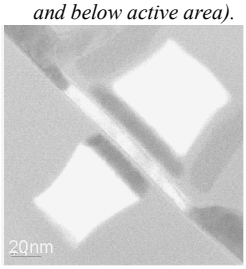


*Fig.6: TEM of 50nm gate length DG MOS with poly-TiN metal gates and NiSi salicided raised S/D.*

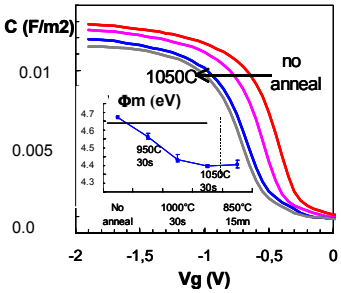


*Fig.7: 2nm $SiO_2$/TiN capacitors for 4 thermal budgets (no anneal, 30s at 950, 1000, 1050°C). Insert: Φm(TiN).*

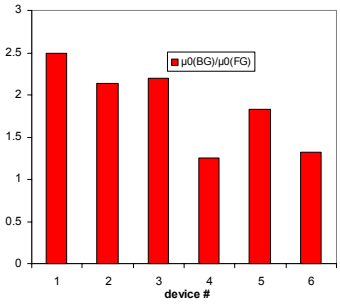


*Fig.8: BG to FG mobility ratio for 100nm DG MOS with oversized BG.*

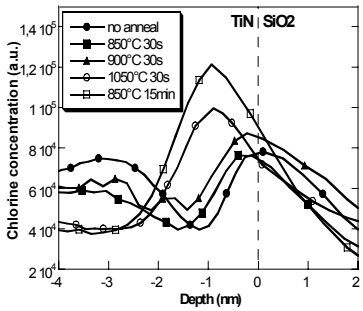


*Fig 9: SIMS profile of Chlorine in CVD TiN for different thermal budgets.*

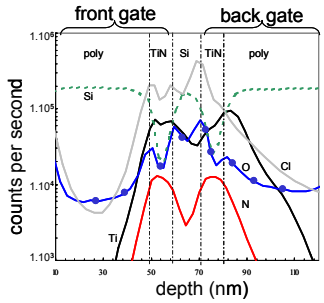


*Fig 10: SIMS profile of the final DG MOS.*

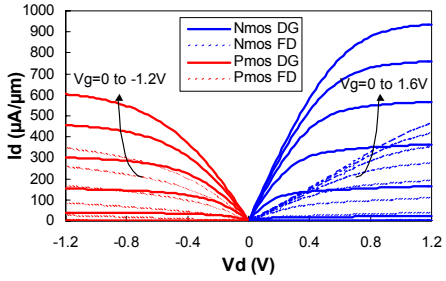


*Fig.11: Output characteristics of 40nm drawn gate length DG and FD transistors.*

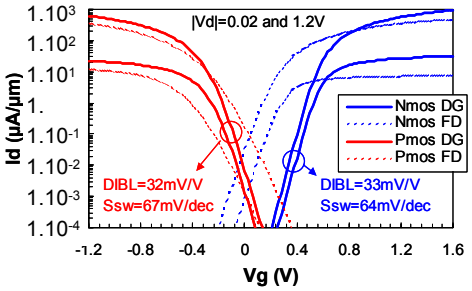


*Fig.12: Transfer characteristics of 40nm drawn gate length DG and FD transistors @ Vd=20mV and 1.2V*

## References


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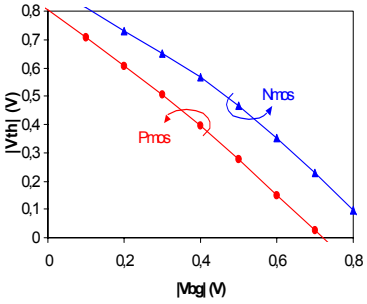


*Fig.13: Tunable threshold voltage of the devices as a function of back gate voltage.*

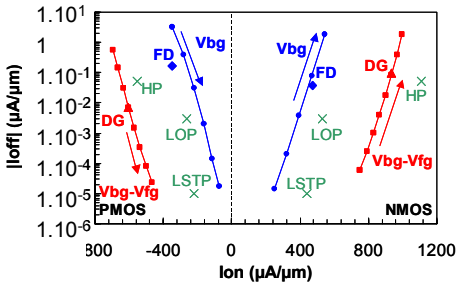


*Fig.14: $I_{off}$ vs $I_{on}$ of tunable DG MOS (adjustable $V_{bg}$-$V_{fg}$) and tunable DG MOS operating in FD mode (adjustable $V_{bg}$) between Low-stand-by-power (LSTP) and High-performance (HP) –90 nm node*