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A Vertical SOI CMOS Technology with p-MOS on Si Film and n-MOS on Bulk Base

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1. Introduction

Three-dimensional (3-D) CMOS technology is one of the most promising candidates for future ULSI application due to its inherent merits such as high density and short interconnection [1]. However, the circuit configuration and material quality of the upper layers are two major challenges. In this work, we demonstrate for the first time a novel 3-D CMOS technology that uses both the Si film and the bulk substrate of a conventional SOI wafer for device and circuit formation. Unlike other proposed 3-D approaches relying on re-crystallized or laterally epitaxial active layers [2], the new one makes the stacked devices to be formed on the in-situ single-crystal layer. With high compact configuration and high performance, the technology offers a new option to increase the circuit density and functionality beyond conventional CMOS scaling.

2. CMOS Configuration and Process

The configuration and layout of the proposed CMOS technology are shown in Fig. 1. As shown, the 3-D CMOS is formed on a conventional SOI substrate with the in-situ single-crystal silicon film for the p-MOSFET (double-gate) and the bulk-silicon base for the n-MOSFET. The n-MOS and p-MOS FETs are distributed vertically, allowing a high compact circuit architecture and over 60% area reduction.

The fabrication process is illustrated in Fig. 2. Conventional SOI wafers are used as starting materials. A modified shallow trench isolations (STI) process is used to define the active area, which begins with growing 15 nm oxide and depositing 20 nm of nitride. A 400 nm shallow trench is opened and a 400 nm LTO film is deposited, followed by planarization with CMP. The exposed nitride is then removed and a 200 nm LTO is deposited [Fig. 2(a)]. After patterning of the LTO/silicon/oxide stack, a 15 nm nitride is deposited as a spacer for the deep source/drain. As+ implantation is performed to dope the source/drain region of the n-MOSFET fabricated at the substrate of the SOI wafer [Fig. 2(b)]. A via hole is opened at the drain region. 500 nm of poly-Si is then deposited and planarized using CMP. The poly-Si is then thinned to about 100 nm in TMAH and the exposed nitride is removed [Fig. 2(c)]. After that, 150 nm of a-Si is deposited and the elevated part is removed by CMP as shown in Fig. 2(d). B+ implantation is performed to dope the source/drain regions of the p-MOSFET and the LTO at the top is then removed in BOE. The active area of the p-MOSFET is then defined and the oxide exposed at the bottom is subsequently removed in BOE as shown in Fig. 2(e). Note that a trench and a tunnel on the top and under the silicon film are formed to self-align the gates to the 3 channels (two for p-MOSFET and one for n-MOSFET). The gate oxides of both n-MOSFET and p-MOSFET are formed by thermal oxidation [Fig. 2(f)], followed by a conformal deposition of 200 nm in-situ doped poly-Si and patterning to form the gate electrode [Fig. 2(g)]. The fabrication is completed with conventional back-end processes [Fig. 2(h)]. The final cross-section from SEM is shown in Fig. 3. It can be seen from the configuration and process that the proposed technology has following features: (1) self-aligned double-gate and thick source/drain of p-MOSFET; (2) 2X channel width of p-MOS; (3) short interconnect distance between devices.

3. Performance

Fig. 4 shows the gate transfer characteristics of the fabricated p-MOSFET and n-MOSFET. The p-MOSFET displays a near ideal sub-threshold slope (~60 mV/dec) due to its double gate structure, whereas the n-MOSFET has a slightly higher sub-threshold swing of 73 mV/dec. Reasonable threshold voltage is obtained and can be adjusted using the doping and gate material. Fig. 5 shows the I_D-V_D characteristics of the p-MOSFET and n-MOSFET. It can be seen that the double-gate p-MOSFET has almost the same current drive as the n-MOSFET with the same lateral width. As a result, the p-MOSFET can be perfectly stacked on an n-MOSFET to form a very compact symmetric inverter. The thick source/drain of the p-MOSFET also provides reasonable reduction in series resistance and the overall source/drain resistance is comparable to that of the n-MOSFET formed on bulk silicon. Fig. 6 illustrates the voltage transfer characteristics (VTC) of the fabricated 3D CMOS inverter. Good transfer characteristics with abrupt transition at both high and low power supply are observed.

4. Conclusions

In summary, a novel 3D CMOS technology, which is featured by fully-self-aligned vertical architecture, double single-crystal device layers and conventional CMOS compatible process is demonstrated. The excellent performances in the fabricated devices and inverter confirm the feasibility of the technology.

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References:

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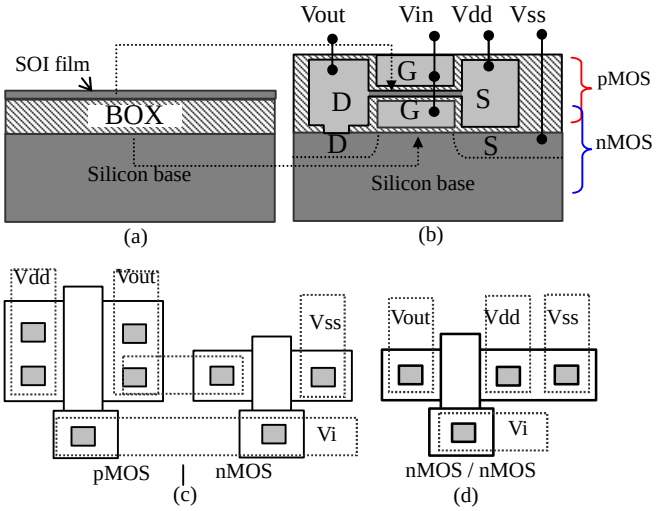
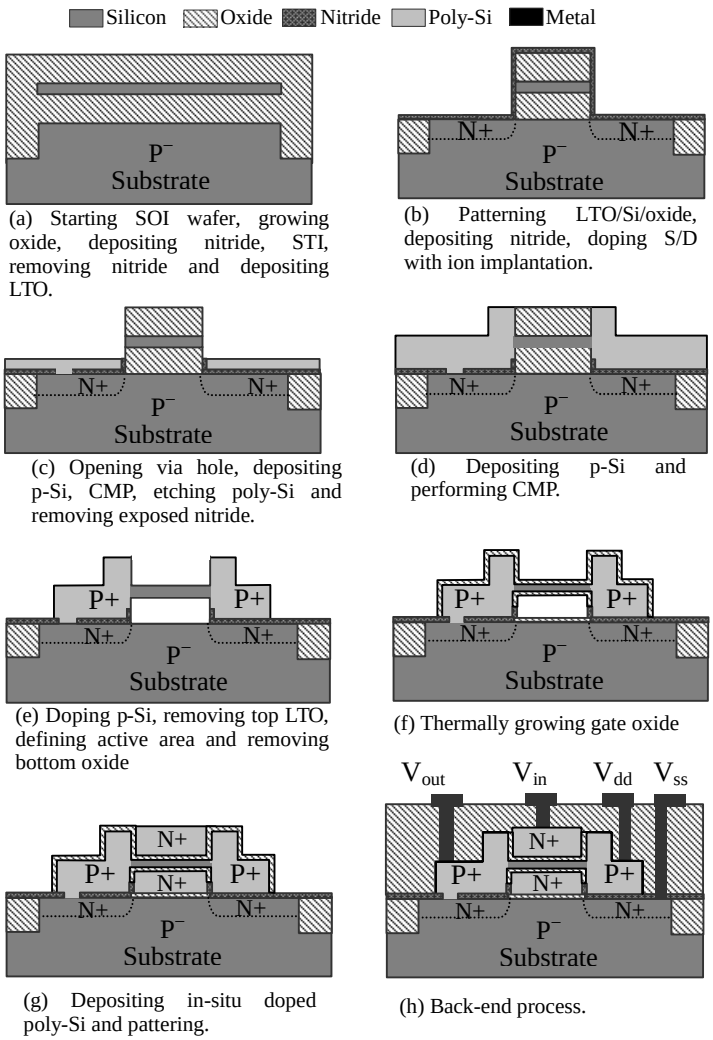


Fig.1 Schematic diagram of the proposed 3-D vertical CMOS technology. (a) Conventional SOI wafer as starting material. (b) Vertical CMOS inverter with double-gate SOI pMOS and bulk silicon nMOS. (c) Layout of a conventional CMOS inverter. (d) Layout of the 3-D vertical CMOS inverter.



(a) Starting SOI wafer, growing oxide, depositing nitride, STI, removing nitride and depositing LTO.

(b) Patterning LTO/Si/oxide, depositing nitride, doping S/D with ion implantation.

(c) Opening via hole, depositing p-Si, CMP, etching poly-Si and removing exposed nitride.

(d) Depositing p-Si and performing CMP.

(e) Doping p-Si, removing top LTO, defining active area and removing bottom oxide

(f) Thermally growing gate oxide

(g) Depositing in-situ doped poly-Si and pattering.

(h) Back-end process.

Fig. 2 Fabrication steps for the proposed self-aligned 3-D vertical CMOS inverter with double-gate SOI p-MOS FET and single-gate bulk n-MOS FET.

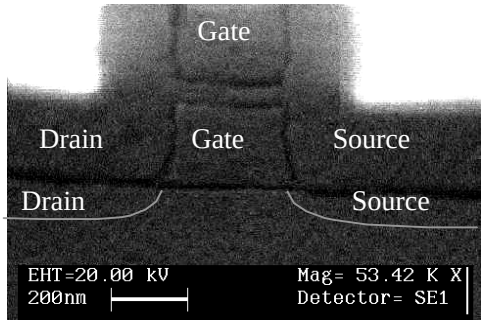


Fig. 3 Cross-sectional SEM photo of a fabricated self-aligned 3-D vertical CMOS structure.

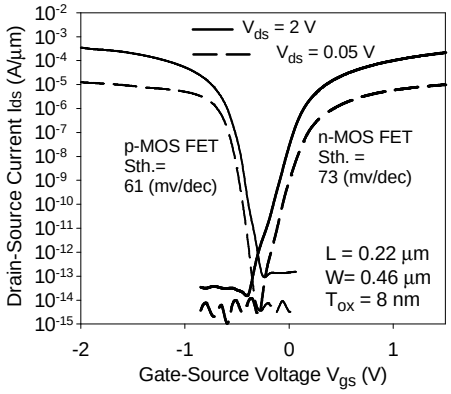


Fig.4 Gate transfer characteristics of the fabricated p-MOS and n-MOS FETs.

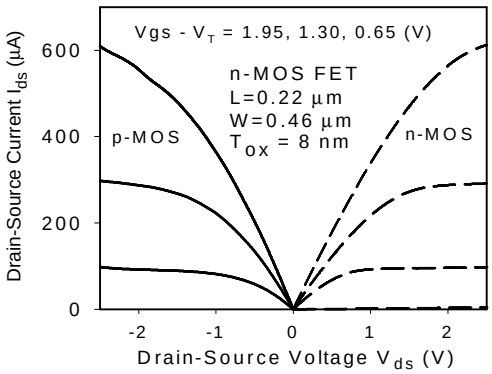


Fig.5 I ~ V characteristics of the fabricated p-MOS and n-MOS FETs.

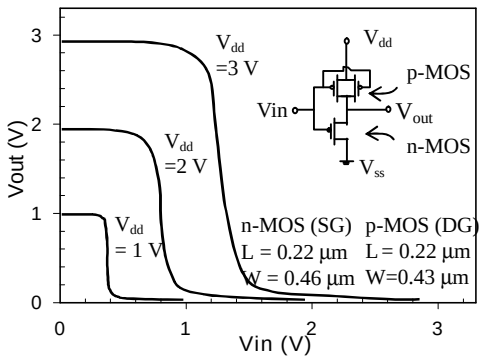


Fig. 6 Voltage transfer characteristics of the fabricated 3-D vertical CMOS inverter.