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A Metallurgical Prescription Suppressing Stress-induced Voiding (SIV) in Cu lines

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1. Introduction

Stress-induced voiding (SIV) has been pointed as a serious issue on the reliability of Cu damascene interconnects as shown in Fig. 1 [1-3]. The Cu interconnects have tensile stress due to the larger thermal expansion than those of the surrounding dielectrics. A void is formed to relax the tensile stress especially at the point connected to an upper line (M2) through via in a lower wide-line (M1). In this paper, mechanism of the SIV under vias has been studied focusing on effects of the Cu characteristics in the upper lines. It is found that SIV in the M1 line is strongly affected by the thermal stress characteristics of the upper line. Suppression of the creep of Cu film in M2 during annealing is a key factor for decreasing the SIV in M1.

2. Experimental

Fig. 2 shows the process and evaluation flow of the test structures. First, M1 layers were fabricated using a conventional Cu metallization in SiO_2. M2 and V1 layers were processed by a dual-damascene scheme, and three kinds of Cu films with barrier layers were applied to them (Table 1). Copper A, B, and C had different characteristics such as the process temperature, the resistivity, and the stress. The via diameter was 0.2μm, and the line width of M1 and M2 was varied from 0.2μm to 10μm. After the M2 copper annealing followed by CMP, the Al-pads on the passivation film were fabricated. These three kinds of wafers were stored up to 2000 hours at 150ºC. The wafer had 56 chips, and the via chain patterns had 10k links. The via chain pattern was defined as a failure, of which resistance was increased 10% higher than the initial value.

3. Results

Fig. 3(a) and (b) are the voltage contrast images of the via chain patterns with 10μm-wide lines. These contrasts represented the open failures in the Cu lines after storing for 2000 hours at 150ºC. Copper A had many contrasts all over the pattern. By the FIB-SEM image at one of the contrast points in Fig. 3(a'), a void was confirmed to grow under the via in the M1 line. Copper B, on the other hand, had only one contrast in Fig. 3(b), indicative of the high resistance to the void formation.

Fig. 4 shows the failure rate of the via chain patterns with Copper A in M2. When M2 was fixed at 10 μm-wide, the failure rate increased drastically with the increment of M1 width over 2μm (Fig. 4(a)). In case of 10μm-wide M1 (Fig. 4(b)), the failure rate reached almost 100% at 2000 hours irrespective of the M2 width. This fact indicates that the voids were formed in the wide M1 lines preferably. The failure rate of the patterns with Copper B, on the other hand, was extremely low irrespective of the line width of M1 and M2 as shown in Fig. 5.

Consequently, it is found that the SIV in the wide M1 is strongly affected by the physical properties of M2 Cu films.

4. Discussion

Stress hysteresis curves of the blanket Copper A and B with the barrier and SiO_2 layer are shown in Fig. 6(a) and (b). The relation between the SIV and the characteristics of M2 copper film is illustrated in Fig. 7. Copper A was deposited at RT, and had compressive stress initially. The compressive stress of Copper A got stronger with temperature increasing due to the mismatch of thermal expansion, and the creep was took place from 100ºC for relaxing the compressive stress. The stress relaxation resulted in the volume contraction at RT. It means that Copper A surrounded with SiO_2 in M2-V1 has the strong tensile stress after annealing, and has given the stress concentration under the via, prompting SIV in the M1 lines. Copper B was deposited at 180ºC, and the initial stress was tensile. The stress of Copper B got compressive at high temperature, but the creep started much higher temperature than that of Copper A. Therefore, the stress relaxation of Copper B was much smaller, resulting in the less volume contraction than that of Copper A.

These results indicate that suppression of the tensile stress in the upper metal, or essentially of the creep during the annealing, is important to reduce the SIV in the lower layers. To confirm our findings, Copper C with smaller thermal expansion and less stress relaxation than those of Copper B was used for M2 Cu film (Fig. 6(c)). As expected, the failure rate was further less compared with Copper B as shown in Fig 8.

5. Conclusions

It is proved that the stress relaxation by the creep of Cu film in the upper lines deteriorates the resistance of SIV in the lower layer. The large tensile stress in the upper lines gives rise to the stress concentration under the via. Control of the metallurgical properties to suppress the Cu creep during annealing is a key factor for decreasing the SIV.

References

[1] E. T. Ogawa, et al., IRPS proc. (2002) 312.
[2] K. Yoshida, et al., Technical digest of IEDM 2002 (2002) 753.
[3] T. Oshima, et al., Technical digest of IEDM 2000 (2000) 123.

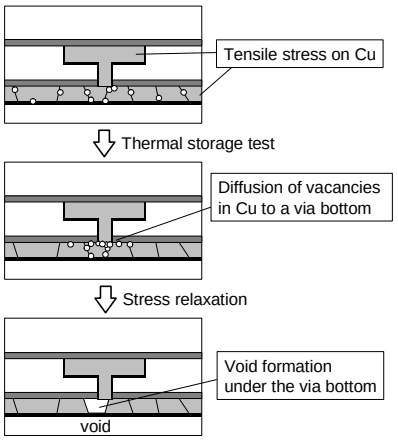

Fig. 1 The schematic diagrams of stress-induced voiding in Cu Metal1.

Table 1 Physical properties of M2 Cu.

	Copper A	Copper B	Copper C
Process temperature (ºC)	RT	180	180
Resistivity (μΩ-cm)	1.70	2.02	2.18
Film stress* (MPa)	63.6	114	110

*The stress of copper/barrier/SiO_2 on Si wafer.

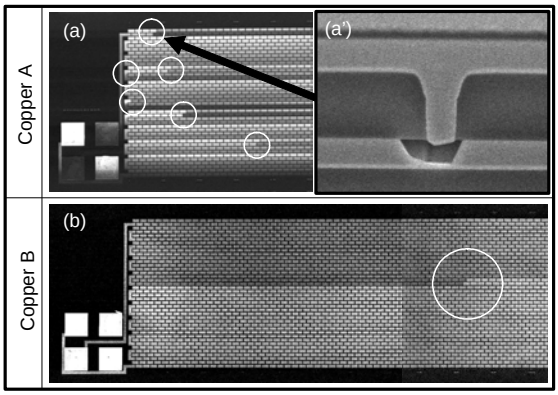

Fig. 3 The voltage contrast patterns of the test patterns with (a) Copper A and (b) Copper B. The FIB-SEM image of a void under the via where the contrast was observed in (a) is shown in (a').

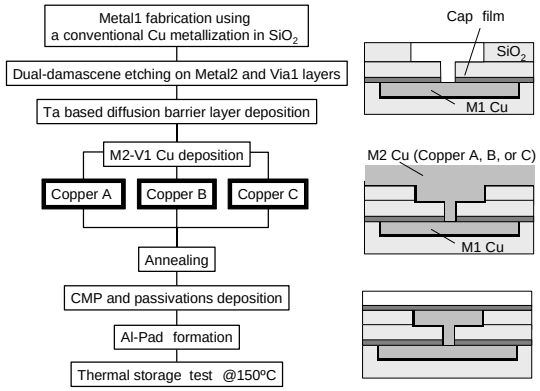

Fig. 2 The process and evaluation flow chart of the test structures.

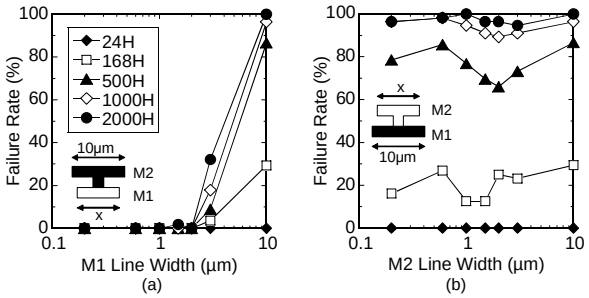

Fig. 4 The failure rate of the via chain patterns of Copper A in M2 as a function of the (a) M1, (b) M2-line width under the stress temperature of 150°C.

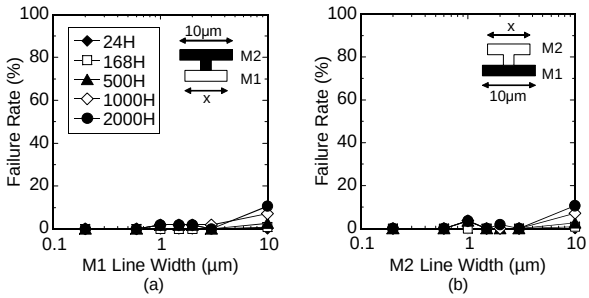

Fig. 5 The failure rate of the via chain patterns of Copper B in M2 as a function of the (a) M1-, (b) M2-line width under the stress temperature of 150°C.

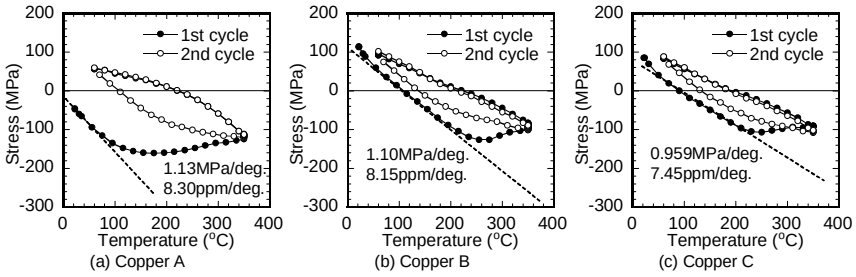

Fig. 6 Thermal stress behaviors of blanket Cu/barrier/SiO_2/Si during the heat cycle. The numbers indicated in graphs represent the thermal stress (upper) and expansion coefficient (lower) of Cu/barrier/SiO_2 on Si wafer.

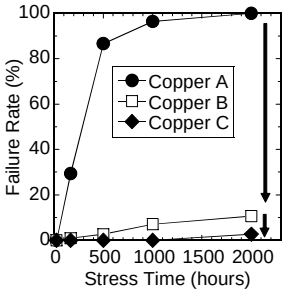

Fig. 8 Stress time vs. failure rate of 10μm wide M1 and M2 line via chain patterns.

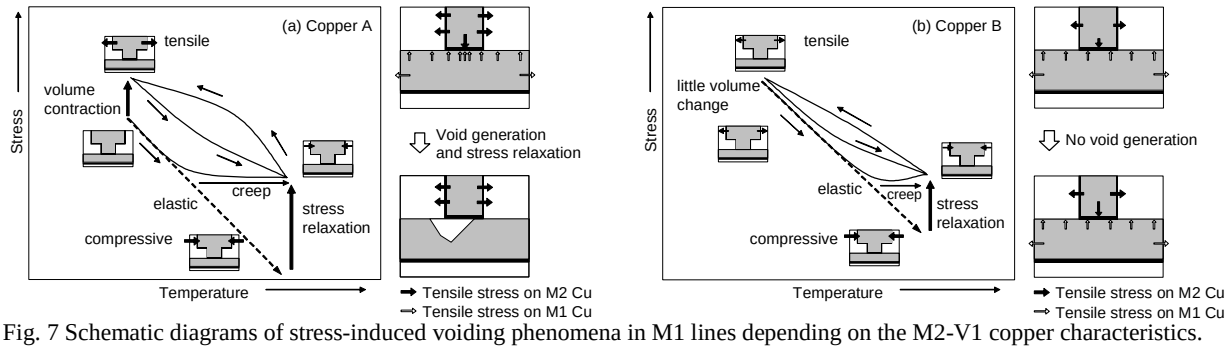

Fig. 7 Schematic diagrams of stress-induced voiding phenomena in M1 lines depending on the M2-V1 copper characteristics.