Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 188-189

B-4-1 (Invited)

Device Design Consideration for 50 nm DRAM Using the Bulk FinFET

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1. Introduction

FinFETs have been considered as a promising candidate for future device technology [1]-[6]. FinFETs built on SOI wafers [1], [2] have been developed mainly for high-speed ICs. FinFETs fabricated on bulk Si wafers have been also reported [3]-[5] and have advantages over SOI FinFETs such as lower wafer price and lower defect density, superior heat transfer rate to the substrate, wide application area, and the suppression of back-bias effect. We call the FinFETs built on bulk wafers the bulk FinFETs, which can be applied to both high-speed ICs and memory technologies including SRAM [4].

MOS devices for sub-100 nm DRAM technology have been suffering from scaling-down problems, and the bulk FinFET can be a solution. In this work, we consider the device design of the bulk FinFET for 50 nm DRAM technology. Using a 3-D device simulator, we investigate device characteristics in terms of the LDD doping profile, S/D to gate overlap length, top oxide thickness, body doping, and fin width.

2. Device Structure and Simulation

Fig. 1 shows the schematic 3-D view of the bulk FinFET. H_G and W_{Fin} stand for the gate height and the fin body width, respectively. T_{FOX} represents the field oxide thickness. x_j is the source/drain junction depth defined as the depth from the top of the fin body. In this work, the H_G and the x_j are fixed at 70 nm and 80 nm, respectively. Gate oxide thickness (T_{ox}) is also fixed at 3 nm. The W_{Fin} is varied. The body is directly connected to the substrate. The cross-sectional view of the bulk FinFET is shown in Fig. 2 (a) in which the top corner is rounded. Fig. 2 (b) shows the cross-section of the bulk-FinFET without the top gate and corners. Figs. 2 (a) and (b) are called the triple-gate (TG) and the ideal bulk-FinFETs, respectively, in this work. Key process steps to fabricate the device are given in ref. [4]. In the 3-D device simulation, key physical models are drift-diffusion (DD) and band-to-band (BTB) tunneling. The DD model can predict the sub-threshold characteristics quite well, but not the on-current (I_{On}) level. It is noted that the GIDL by the BTB model seems to be higher than anticipated.

3. Results and Discussion

Figs. 3 (a) and (b) show device characteristics of the TG bulk FinFET with constant source/drain (S/D) LDD doping concentration. As the LDD doping decreases, I_{Off}, DIBL, and SS are improved. Here, the fin body doping is $5x10^{18}$ cm^{-3}. The gate to S/D non-overlap structure can improve device scalability [6]. V_T and I_{Off} with the gate overlap length (L_{ov}) are shown in Fig. 4. The "-" in the L_{ov} represents non-overlap. We think that the 0 to –3 nm L_{ov} is reasonable since too much non-overlap degrades I_{On}. If we increase the top T_{ox} from 3 nm to 10 nm, the device looks like double-gate as shown in Fig. 5. Thicker top T_{ox} increases V_T, but GIDL is nearly the same. We can observe the DIBL degradation with the thick T_{ox}, because the effect from corner regions becomes small, as will be explained later. The doping level in the top corner region of the fin body is very important in suppressing I_{Off}. V_T and I_{Off} with the doping level are shown in Fig. 6. About 30 % higher doping in the fin top than the constant body doping looks better for low I_{Off}.

Fig. 7 shows the I_D-V_{GS} characteristics as parameters of the W_{Fin}, body doping, and gate work function. With decreasing W_{Fin}, minimum I_D decreases, but saturates after full depletion of the LDD (here, W_{Fin} of 15 nm). Under the same condition as the ones in Fig. 7, V_T and DIBL with W_{Fin} are shown in Fig. 8. The DIBL improves significantly with decreasing W_{Fin}, and the device with low body doping ($5x10^{18}$ cm^{-3}) and mid-gap work function shows worse DIBL since the low body doping enhances the bulk punch-through.

Fig. 9 shows V_T and DIBL of the TG and the ideal bulk FinFETs with the peak Gaussian doping concentration at the edge of the fin body for LDD. The doping at the center of the fin body is about 20 times lower than that of the peak doping. The TG bulk FinFET has much lower V_T due to earlier conduction along the corner regions. Since the DIBL is mainly affected by the low V_T corner-parasitic-channel in which the DIBL is lower, the TG bulk FinFET shows lower DIBL. Figs. 10 and 11 show V_T, I_{Off}, DIBL, and SS versus LDD doping ratio. The LDD peak concentration ($N_{LDD(peak)}$) is fixed at $7x10^{19}$ cm^{-3} and located at the edge of the fin body for the S/D. The LDD doping at the center of the fin body varies. The doping profile from the edge to the center is Gaussian. The ratios larger than about 10 are considered to be reasonable.

4. Conclusion

We have considered the bulk FinFET design for 50 nm DRAM technology. Challenging methods to improve I_{Off} and DIBL are the doping concentration increase near the top of the fin body, LDD doping concentration decrease, thinner fin body, Gaussian LDD doping profile with peak concentration at the edge of the fin body for source/drain.

Acknowledgements

This work was supported by Tera Level Nanodevices Project of MOST in 2004.

References

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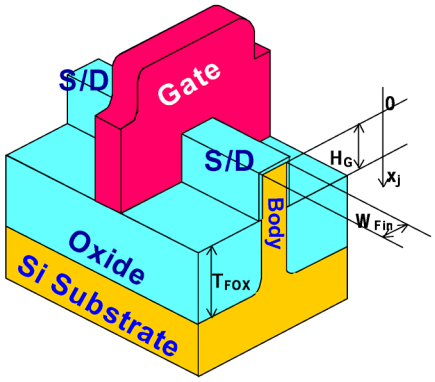
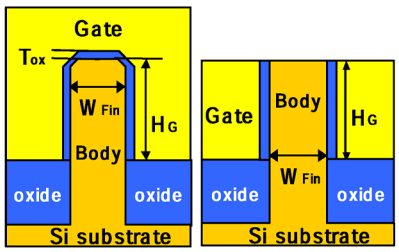


Fig. 1. Schematic 3-D view of the bulk FinFET. H_G and W_{fin} stand for the gate height and fin body width, respectively. The x_j is source/drain junction depth defined as the depth from the top of the fin body.



(a) (b)

Fig. 2. Schematic cross-sectional views along the gates for (a) the TG, and (b) the ideal bulk FinFET without the top corner regions of the fin body.

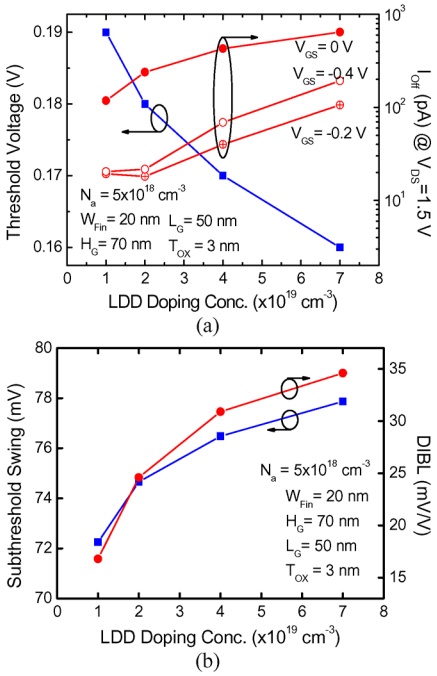


Fig. 3. V_T, I_{Off}, subthreshold swing (SS), and DIBL characteristics versus constant LDD concentration. W_{fin} and T_{ox} are 20 nm and 3 nm, respectively. The body doing is 5x10^{18} cm^{-3}.

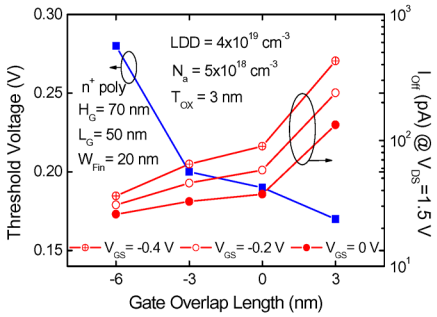


Fig. 4. V_T and I_{Off} versus gate overlap length. I_{Off}s were captured at V_{GS} biases of -0.4, -0.2, and 0 V.

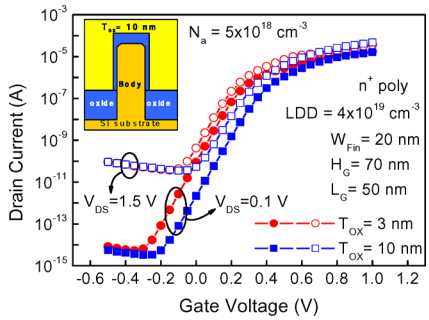


Fig. 5. I_D-V_{GS} characteristics as a parameter of top gate oxide thickness. The square symbols represent the data for the oxide thickness of 10 nm.

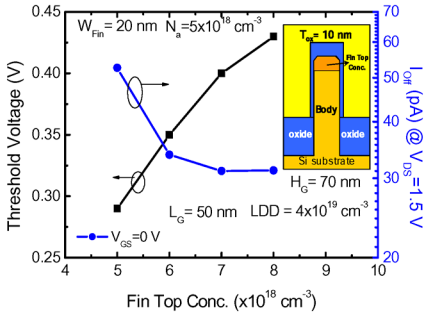


Fig. 6. V_T and I_{Off} versus the doping concentration in the fin top region. The insert shows high doping region near the fin top on the cross-sectional view of the fin body.

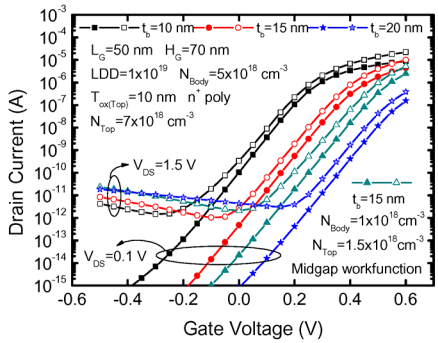


Fig. 7. I_D-V_{GS} characteristics as parameters of fin body thickness and body doping. The triangular symbols represent the data for the device with the low body doping and the mid-gap work function.

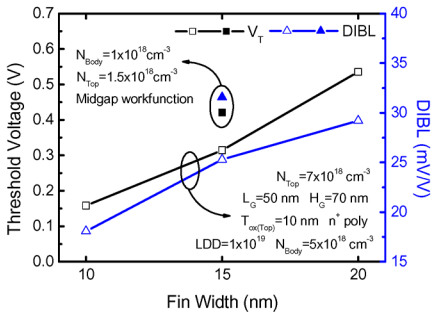


Fig. 8. V_T and DIBL characteristics with the fin width. The solid symbols represent the data for the device with the low body doping and the mid-gap work function.

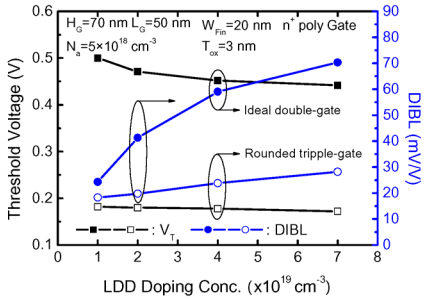


Fig. 9. V_T and DIBL versus LDD concentration as a parameter of device structure. The ideal double-gate device does not have corner regions as shown in Fig. 2 (b).

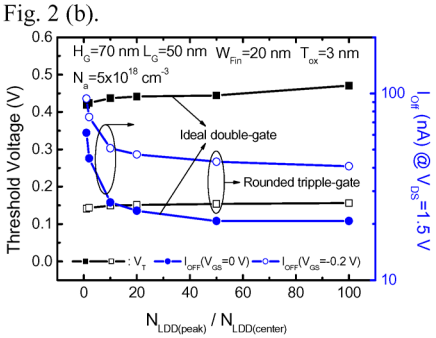


Fig. 10. V_T and I_{Off} versus LDD doping ratio. The LDD peak concentration ($N_{LDD(peak)}$) is fixed at 7x10^{19} cm^{-3} and located at the edge of the fin body for the S/D. The LDD doping at the center of the fin body varies. The doping profile from the edge to the center is Gaussian.

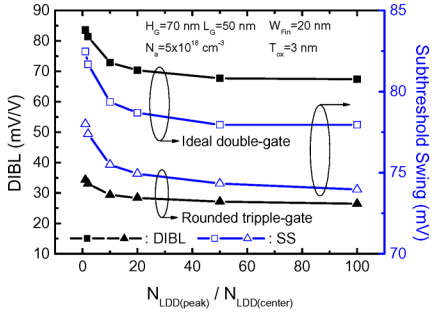


Fig. 11. DIBL and SS versus LDD doping ratio. The LDD doping profiles are the same as the ones in Fig. 10.