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Highly Manufacturable 64M bit Ultra Low Power SRAM Using a Novel 3-Dimensional S^3 (Stacked Single-crystal Si) Cell Technology

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1. Introduction

Due to the great demands for higher density SRAM in all area of SRAM applications, such as mobile, network, cache, and embedded applications, aggressive shrinkage of 6T full CMOS SRAM had been continued as the technology advances. Nevertheless, the number of transistors per cell has been a basic limitation in the further shrinkage of the SRAM cell size. In order to save the cell area, as one of alternatives to the 6T full CMOS, the poly Si TFT (Thin Film Transistor) load SRAM and 4T cell with poly-Si resistor loads cell had been widely used for low power applications [1] and high speed applications [2], respectively. In spite of the area saving advantages of the both cell types compared to the 6T full CMOS cell , they could not replace the 6T full CMOS because they are basically much inferior in the respects of the low power consumption, the low voltage operation, and the high speed characteristic due to poor electrical properties of the load devices made of poly Si films. Therefore, to overcome the poor electrical characteristics of the TFT load PMOS and reduce the SRAM cell size without the lithographic shrink, the S^3 (Stacked Single-crystal Si) SRAM cell with stacked cell transistors, the so-called SSTFT (Stacked Single-crystal Thin Film Transistor), was developed [4].

In this work, we present the highly manufacturable 64Mb SRAM for low power applications using 80nm S^3 cell technology and stacking process of the single crystalline thin film transistors on the ILD.

2. Process Integration

Cell layout and Vertical Structure

The S^3 cell is made up with 2 layers of transistors; the pull-down and access transistors are made on the bulk Si (Fig.1) and the load pMOS SSTFT of the SRAM cell is formed on the upper layer (Fig.2), which is on the ILD layer and the bulk Si transistors. Figure 3 shows the top view image of node contacts, which connect the cell transistors between the bottom and upper layers. The detailed fabrication process flow is summarized in Table 1. For $46F^2$ SRAM cell with $0.294um^2$ area, the critical dimension of each pattern is shown in Table 2. Figure 4 shows the cross sectional STEM image of the single stacked S^3 SRAM cell arrays.

Load pMOS SSTFT

The crystal quality of the silicon channel of SSTFT is one of the most important factors for electrical characteristics of the load PMOS SSTFT in S3 cell. The load pMOS SSTFT on ILD (Inter Layer Dielectrics) has a single crystalline silicon channel as shown in HRTEM image (Fig.5). Figure 6 shows the Raman spectra of the various Si films analyzed with Raman spectroscopy. The peak of the channel Si is well matched with one of single crystal Si . In spite of some crystal defects, such as the stacking fault and twins, the electrical characteristics of SSTFT are comparable with those of bulk Si Tr. as shown Fig.7. The sub-threshold swing (140mV/dec. at 85°C) and the on current above 1uA at Vds = -2.0V are good enough for the load transistor of low power SRAM cell.

Contact formation with side wall

The more aggressive scaling of S^3 cell size could be possible by the formation of sidewall node contacts. For the formation of latch of SRAM cell, interconnection between the bulk pull-down and the load PMOS on ILD is necessary. As shown in Fig.8, the stable contact was formed between the active node and the drain of load SSTFT through the sidewall of contact. The resistance of the sidewall contact (*Rsc*) is very sensitive to the process conditions, especially the doping level and the cleaning method before contact-filling. By optimizing the process conditions, a good distribution of the *Rsc* with the value of ~1Kohm/contact has been obtained as shown in Fig.9.

3. Device characteristics

With the $0.294um^2$ SRAM cell technology based on the stacking process and the load PMOS SSTFT, 64Mb low power SRAM was fabricated successfully as shown in Fig.10. The distributions of stand-by current of the 64M bit SRAM are shown in Fig.11. The access time (tAA) is less than 55nsec (Fig. 12) at 85°C, Vdd = 2.0V. These characteristic values are comparable with those of the low power SRAM fabricated with the 6T full CMOS cell.

4. Conclusions

With the load SSTFT and the sidewall contact, we could scale down aggressively the SRAM cell size to $46F^2$ and fabricate successfully a 64M bit low power SRAM.

This S^3 cell technology has made an epoch for shrinkage of SRAM cell size. Near future, this technology will be extended to multi-stack technology which is competitive in ultra high density applications of SRAM.

References

[1] T. Yamanak *et. al*., *IEDM Tech. Digest*. (1990) 477.
[2] C. Lage, et al, *IEDM Tech. Dig*, (1996) 271.
[3] Soon-Moon Jung *et al*., *IEDM Tech. Dig*., (2003) 289.
[4] Soon-Moon Jung *et al*., 2004 Symposium on VLSI Technology, to be published.

Table 1 Detailed process flow of S^3 SRAM

- Active (shallow trench isolation)
- Well & Vth adjust implantation
- 1st gate oxidation
- Bulk pull-down, pass, peripheral Tr
- Halo/LDD Implant , 1'st Spacer and S/D implant
- 1st ILD/ILD CMP
- ***Formation of single crystal channel Si for load pMOS SSTFT***
- 2nd gate oxidation
- Top gate poly for load pMOS SSTFT
- Halo/LDD implant and 2nd Spacer
- Blank p+ S/D implant and RTA
- 2nd ILD/ILD CMP
- NC1 and NC2 formation

Table 2 Critical dimension of single stack $46F^2$ S^3 SRAM

Item	Dimension
Cell size	0.294 um^2
Isolation Pitch	220nm
Active Region Minimum Pitch	240nm
Bottom Gate Minimum Pitch	260nm
Channel Si Pitch of load pMOS SSTFT	240nm
Top Gate Pitch	170nm
Minimum contact size (Bottom CD)	80nm
Minimum contact pitch	260nm
Bit line pitch	224nm

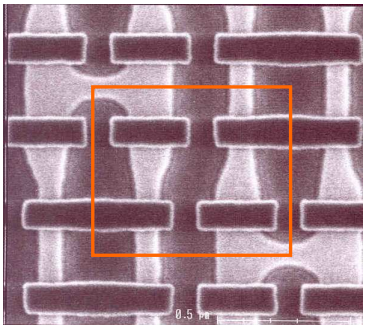

Fig.1 Top view SEM image of the active region and Bulk Transistors

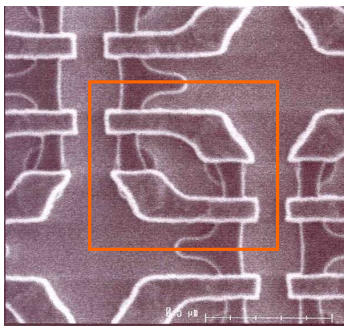

Fig.2 Top view SEM image of the Channel Si and SSTFT top gate

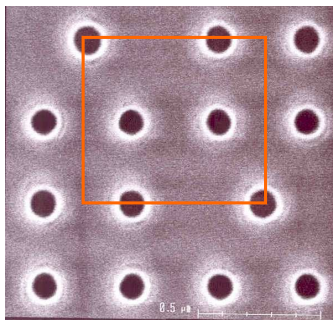

Fig.3 Top view SEM image of the Node contact layer in S^3 cell

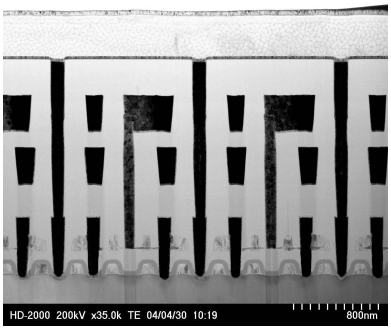

Fig.4 Cross sectional SEM image of the Single stack S^3 SRAM cell

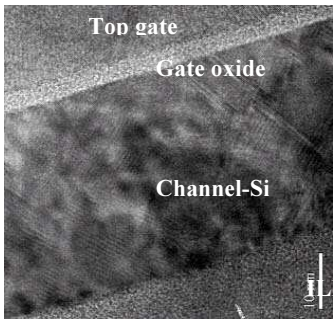

Fig.5 High resolution TEM image of the channel Si crystal

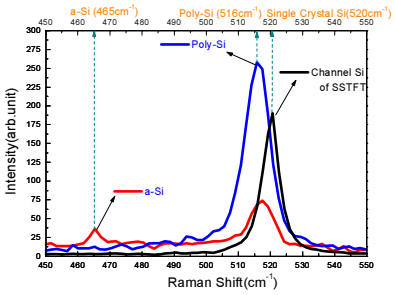

Fig.6 Raman spectra of the channel Si crystal in the load PMOS SSTFT

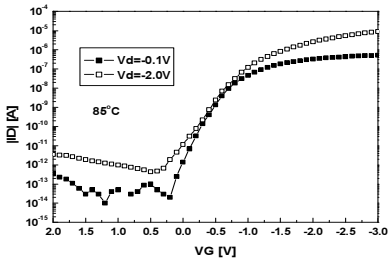

Fig.7 Current characteristics fo the load PMOS SSTFT measured st 85℃

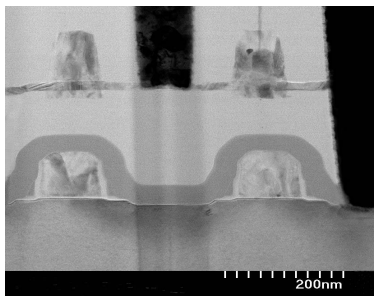

Fig.8 Cross sectional SEM image of vertical node contact with the side wall of W plug

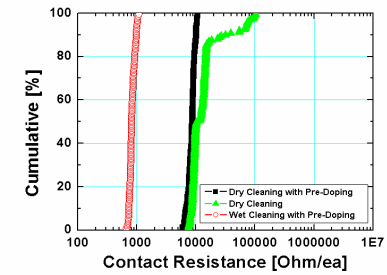

Fig.9 Contact resistance distribution of Node to top gate of load PMOS SSTFT

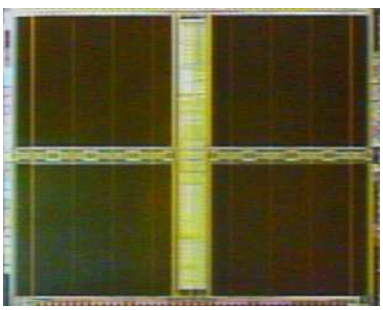

Fig.10 A photograph of fabricated 64M bit SRAM

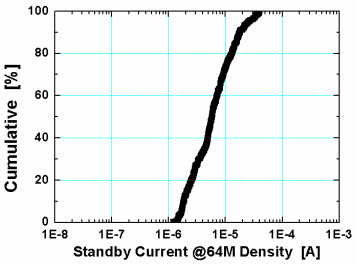

Fig.11 Standby distribution of the 64M bit SRAM with single stack S^3 cell

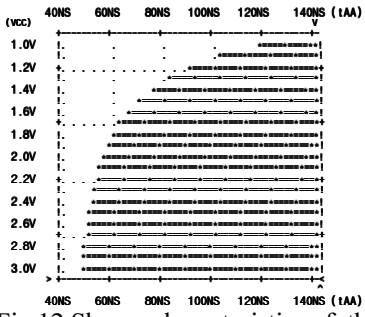

Fig.12 Shmoo characteristics of the 64M bit SRAM with single stack S^3 cell