Re-examination of Impact of Intrinsic Dopant Fluctuations on SRAM Static Noise Margin

Fumihiko Tachibana and Toshiro Hiramoto

Institute of Industrial Science, University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan Phone: +81-3-5452-6264 Fax: +81-3-5452-6265, E-mail:fumihiko@nano.iis.u-tokyo.ac.jp

1. Introduction

With scaling of MOSFET dimensions, variations of CMOS characteristics due to random dopant fluctuations [1] as well as size variations have become larger and larger. The variations have a great impact on SRAM Cell Static Noise Margin (SNM), leading to the degradation of yield.

The deviations in SNM due to dopant fluctuations have been intensively investigated [2]. This paper has warned that four sigma of deviations in SNM due to intrinsic fluctuations alone exceeds the average SNM and the yield is severely degraded when L_g=50nm. However, parameters assumed in Ref. [2] were based on 1997 NTRS where V_{dd} was very low (0.5V) and W_g equals to L_g, which is significantly different from 2003 ITRS [3]. They assumed the worst condition of small β ratio (β =1) and very high temperature (400K). Moreover, they utilized an analytical model of SNM that had many approximations and ignored the body effect. Thus, more precise evaluations using realistic parameters are strongly required.

In this paper, average SNM (SNM_{ave}) and σ SNM at 298K for several technology generations based on 2003 ITRS are calculated using SPICE simulations. It is shown that five sigma of SNM deviations is ensured at L_g=53nm in 90nm node. It is also demonstrated that, although σ SNM rapidly increases in 65nm and 45nm nodes, four sigma of SNM is ensured even in 45nm node by adjusting L_g, V_{dd}, V_{th} and DIBL.

2. Method

Fig. 1 (a) and (b) show the definition of SNM and the circuit schematic of a SRAM Cell, respectively. First, σV_{th} due to dopant fluctuations is calculated by the cube model [2][4] using the device parameters in Table 1, where T_{oxe} is the electrical oxide thickness. N_A is obtained by 2D device simulator [5]. Second, SNM of SRAM Cell is calculated by SPICE simulations. The SPICE model used is UCB's PTM [6], and we have modified to follow device characteristics of low-operation-power (LOP) devices in 2003 ITRS. Changing V_{th} of one transistor, the sensitivity of SNM to variations in V_{th} of each cell transistor is obtained, as shown in Fig. 1 (c). Finally, joint σ SNM (when all transistors are independently fluctuated) is obtained by,

| $\sigma SNM_L = \sigma V_{th}$ | $\left(\frac{\partial SNM_{nR}}{\partial V_{T_{nR}}}\right)^2 +$ | $\left(\frac{\partial SNM_{nL}}{\partial V_{T_{nL}}}\right)^2 +$ | $\left(\frac{\partial SNM_{pR}}{\partial V_{T_{pR}}}\right)^2 +$ | $\left(\frac{\partial SNM_{aL}}{\partial V_{T_{aL}}}\right)^2$ |
|--------------------------------|------------------------------------------------------------------|------------------------------------------------------------------|------------------------------------------------------------------|----------------------------------------------------------------|
| | | | | |

3. Results

Fig. 2 shows distribution density functions of SNM due to intrinsic V_{th} fluctuations at β =1 and 1.5. Obtained values of SNM_{ave} and σ SNM are summarized in Table 2. At L_g=53nm in 90nm node, 5 sigma of SNM is ensured (SNM_{ave}/ σ SNM > 5) at β =1.5. However, SNM_{ave}/ σ SNM is

less than 4 in 65nm (L_g =32nm) and 45nm (L_g =22nm) nodes.

To keep high yield in 65nm and 45nm nodes, it is strongly required to increase SNM_{ave} and suppress σSNM . The cell design to obtain high $SNM_{ave}/\sigma SNM$ is discussed in the following. Fig. 3 (a) and (b) show the dependence of SNM_{ave} on V_{dd} and V_{th} , respectively, indicating that changing both V_{dd} and V_{th} is important to raise SNM_{ave} effectively. It is found that DIBL greatly affects SNM_{ave} . Fig. 3 (c) shows the DIBL dependence of SNM_{ave} , where it is assumed that V_{th} at $V_{ds}=V_{dd}$ is constant and only DIBL is changed. V_{th} at low V_{ds} in MOSFET with high DIBL is higher than that of MOSFET with low DIBL. This makes a difference in butterfly curves, as shown in Fig. 4. In order to keep SNM_{ave} high, DIBL should be suppressed.

L_g in LOP devices in 2003 ITRS is too aggressively scaled for SRAM applications. Another method to obtain high SNM_{ave}/ σ SNM is to relax the L_g scaling. Fig. 5 shows L_g dependence of N_A and σ V_{th} with constant V_{th}. As L_g becomes longer, the short channel effect is suppressed, resulting in lower N_A and smaller σ V_{th}. Thus, σ SNM can be suppressed. Fig. 6 shows the distribution density functions of SNM using adjusted parameters, where L_g=30nm, N_A= 4.45x10¹⁸ cm⁻³, DIBL=80mV/V, V_{dd}=0.8V, and V_t^{sat}=0.25V. The result indicates that SNM_{ave}/ σ SNM is larger than 4, and four sigma of SNM can be ensured even in 45nm node by adjusting parameters. It should be noted that we considered the effect of dopant fluctuations alone. When size variations are taken into account, higher SNM_{ave} is required.

4. Conclusions

SRAM SNM_{ave} and σ SNM due to dopant fluctuations alone are re-examined based on LOP devices in 2003 ITRS using SPICE simulations. It is shown that 5 sigma of SNM is ensured in 90nm node at β =1.5 and 4 sigma is ensured even in 45nm node by adjusting Lg, V_{dd}, V_{th} and DIBL.

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Table 1. Input parameters for simulations [3].

Fig. 4. Butterfly curves for MOSFETs with two different DIBL in 45nm node at β =1.5.

Fig. 5. L_g dependence of N_A and σV_{th} . Black and white symbols indicate N_A and σV_{th} , respectively.

Fig. 6. Distribution density functions of SNM after adjusting parameters. Four sigma of SNM is ensured in 45nm node at β =1.5.